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SINGLE PHASE INVERTER FOR A THREE PHASE
POWER GENERATION AND DISTRIBUTION SYSTEM

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ABSTRACT

The purpose of this contract was to develop a breadboard design of a single-phase inverter with sinusoidal output voltage for a three-phase power generation and distribution system. This study was performed by Dr. S. Lindena of Xerox/Electro-Optical Systems. Dr. G. Wester of the Jet Propulsion Laboratory was the technical monitor.

The three-phase system will consist of three single-phase inverters, whose output voltages are connected in a delta configuration. Upon failure of one inverter the two remaining inverters will continue to deliver three-phase power. Parallel redundancy as offered by two three-phase inverters is substituted by one three-phase inverter assembly with a high savings in volume, weight, components count and complexity and a considerable increase in reliability.

To accomplish this goal this study proved that a current-fed single-phase sinusoidal inverter meets all of the technical requirements to accomplish above stated operational requirements.

These requirements are:

1. Each single-phase, current-fed inverter must be capable of being synchronized to a three-phase reference system such that its output voltage remains phaselocked to its respective reference voltage.

2. Each single-phase, current-fed inverter must be capable of accepting leading and lagging power factors over a range from -0.7 through 1 to +0.7

3. Each single phase current-fed inverter must deliver a regulated sinusoidal output voltage with a total distortion of less than 10 percent under various conditions of load power factor, load level, load changes and input voltage variations.

The study was performed on a single-phase inverter only as each of the three inverters in a three-phase system must have identical characteristics and must be capable of maintaining operation with respect to its reference phase only. No master-and-slave phase relation is being used and allows upon failure of any one inverter to maintain a three-phase system.

This report also presents the design equations for a current fed inverter and describes the operation of the power stage and the control circuit. It furthermore derives the operational requirements of single-phase inverters which operate in a three-phase system with all three inverters or only two inverters in operating condition.

From the theoretical and experimental investigations the following conclusions can be drawn:

1. The current-fed sinusoidal inverter is capable of both delivering a sinusoidal output voltage and without preloading can operate into any power factor over the full range from a 90 degree leading to a 90 degree lagging power factor.

2. It can maintain virtually zero phase lock position with respect to a synchronizing reference signal and each inverter can therefore operate independently from a normally required master phase.

3. In an open V connection the current-fed inverter can supply a three phase system.

4. Failure of any one phase allows to maintain an operational three phase system and a block redundant system is not required.

5. The current-fed inverter is an efficient conversion approach. Efficiency, however, drops with an increase of input voltage swing and with lower power factors.

CONTENTS

CONTENTS (Contd)

ILLUSTRATIONS

INTRODUCTION

Spacecraft power distribution systems must have a high degree of reliability and hence a rather low failure rate. If a failure does occur the objectives of the spacecraft mission may not be achievable at all or only partial objectives may be accomplished. The general approach in overcoming this problem has been in the use of stand-by, block redundant, systems. This simply implies that a complete conversion system of full power capability is carried along and is ready to take over all functions of the failed "box." This approach does work satisfactorily and therefore has been the main approach. The penalties for this approach, however, are quite severe if we consider that space and weight are twice as much as that of one system. There have been, and there still are, under investigation some "self-healing" systems which are capable of replacing a failed part or sub-circuits only. Due to the complexity and magnitude to which "spare circuits" were carried along, this approach so far has not gained much favor.

Another approach using parallel redundancy has been implemented successfully and appears to offer several advantages if it can meet some additional conditions:

1) In a conversion system which consists of two or more parallel operating converters the failure of one converter should not disable the conversion system completely but should be capable of continuing to operate at a reduced power capability.

2) If possible the failed converter which delivered part of the full power should be replaced by a stand-by converter. In the case of two parallel converters one carries a spare part with a capability of 50% of the total power. In a converter or inverter with three conversion channels one would carry only one spare channel with a capability of only one third of the total power requirement.

It becomes apparent that this approach can be lighter than two complete block redundant systems and yet offers the same reliability.

The theoretical and experimental investigation into the capabilities of the single phase current-fed inverter proved that this inverter can indeed maintain a three-phase distribution system even if any one of the three phases (inverters) fails. The key to the performance, is the capability of the current-fed inverter to handle any power factor, maintain a sinusoidal waveshape and shift the base drive in such a manner that upon application of any power factor the output voltage remains in phase with a reference phase.

As each of the three phases has its own reference phase no master channel is required and any one phase may fail resulting in an open V-connection which is still capable of delivering three-phase power.

These performance requirements of the current-fed inverter have been investigated, studied and verified on a single phase inverter and yield a solid basis for follow-on work on a complete three-phase system.

SECTION 1

THE GOAL AND THE PERFORMANCE PREREQUISITES

The goal for a three phase distribution system is the capability upon loss of one phase to maintain three phase operation at reduced output power.

In a three phase power generation and distribution system, several combinations of connections on the primary and the secondary side are possible. The following connections are possible:

a) Star-Star
b) Star-Delta
c) Delta-Star
d) Delta-Delta

Furthermore, the individual phases can be contained on three single phase transformers or on one three phase transformer. In addition in any star connection one may consider a three wire (Neutral floating) or a four wire system (Neutral fixed or floating). Under the assumption that upon failure of one phase the system must remain operative, only two output connections are meeting this requirement. They are the four wire star with fixed neutral and the delta output connection. Of these two connections let us pay some closer attention to the latter one: the delta output connection. Figure 1-1 shows the voltage vector diagrams of a three phase system with three individual transformers (3 channel, 3 phase system). On the left side all three phases are active. On the right side, phase C failed and is missing. As the secondary vector diagram shows phases A and B maintained voltage and phase relation but vector C is now the vector sum of phase A and B and though the magnitude is the same, the phase relation of phase C has changed by 180° as shown in dashed lines. As far as the outside is concerned the three phase system is still fully available at the "corners of the vector triangle." The only difference appears to be that no longer three channels but rather two channels in a V-connection (vectors A and B on the secondary side) establish the three phase system. The total available power will therefore decrease by at least the power of one channel.

There is, however, a much more important change which can best be understood if we connect a resistive load across the dashed-line phase in figure 1-1, lower right side. This is, of course, a condition which will rarely exist as normally some load will be present on the other phases, but it lets us see immediately a requirement which any inverter has to meet if it operates in the open V configuration.

A resistive load across the dashed voltage vector C causes a current flow in phase with this voltage; i.e., as the voltage vector is shown @ $+120^{\circ}$, the current vector will also have a phase @ $+120^{\circ}$ polar angle. This current is, however, delivered by the phase voltages A and B which at this moment have polar angles of $+60^{\circ}$ and $+180^{\circ}$, respectively. As the <u>resistive</u> current has at this moment a phasing of 120° it shows that phase A is carrying this current with a lagging angle of 60° and phase B carries this current with a leading angle of 60°.

If one assumes that under the same conditions as above (phase C disabled) three resistive and equal loads are connected across the remaining two active phases A and B and the inactive phase C, then phases A and B each will deliver equal current at a magnitude 1.73 times larger than the resistive current. In the case of phase A this current will lag the phase voltage by 30° and in the case of phase B this current will lead the phase voltage by 30°. In both cases a resistive load causes leading and lagging power factors and an overload of 73% in the two remaining active phases. Derating is therefore required.

From these observations we learn the important requirements that a three phase power generation and distribution system which must be capable of maintaining derated operation upon failure of one phase or channel <u>must</u> have the following inherent characteristics:

a) It must maintain the phase displacements.

b) Each phase must be capable of handling both leading and lagging power factors.

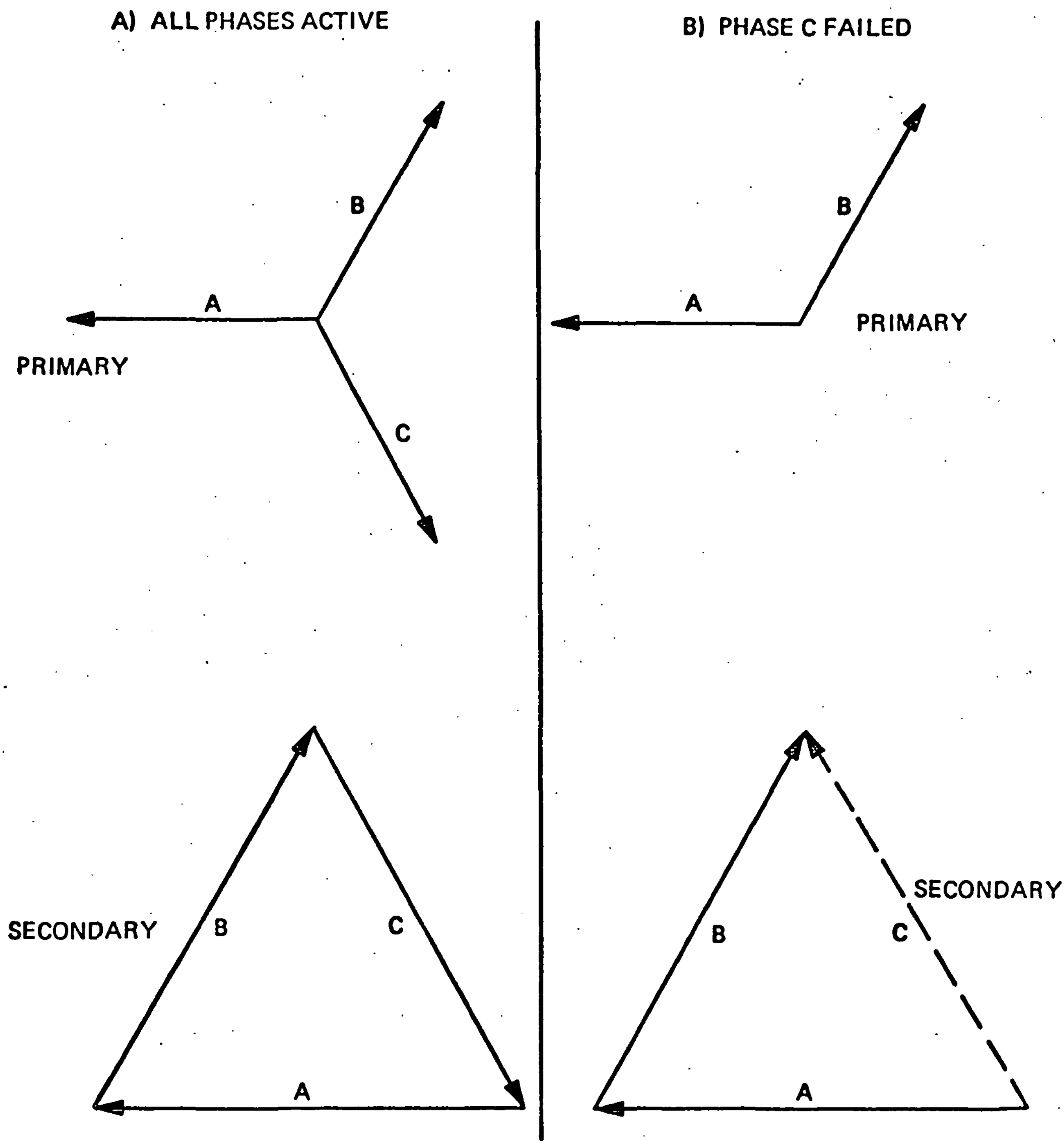


Figure 1-1. Vector Diagram of a 3ϕ System λ-Δ With and Without Loss of one Phase.

52352

c) In case of failure of one phase the remaining phases must be protected against overload.

d) In the case of pure resistive load on all three phases, sinusoidal voltages and currents, and upon failure of one phase the total power capability will be reduced by a factor of $\sqrt{3}$.

e) If the voltages are sinusoidal and if pulse-width modulation is used to generate and regulate these voltages, additional output power derating is required upon failure of one phase. (The reason for this is an increase of input rms current as function of power factor.)

Of all above mentioned requirements, the capability of handling any power factor is the most important one. It is, therefore, advisable to investigate and compare the capabilities of the two types of inverters. These two types of inverters are

a) the voltage-fed inverter
b) the current-fed inverter.

SECTION 2

DESIGN CONSIDERATIONS

This section contains the analyses and design considerations of the two basic static inverter types which are presently used in inversion circuits. The two inverter types considered are:

a. Voltage-fed
b. Current-fed

These terms are defined as follows:

a. A voltage-fed inverter is any inverter in which the design of the circuit connects the dc voltage source through semiconductor switches, directly to the primary of the transformer.

b. A current-fed inverter is any inverter in which the design of the circuit forces a constant current to flow through the semiconductor switches and through the primary of the transformer during the full conduction period of the switches; regardless of the source voltage waveform, the load variations, or the power factor conditions.

The current-fed inverter was considered for the feasibility study to solve two significant problems.

1. The current-fed inverter can handle power factor

   It can be designed to operate into any power factor load that varies from leading to lagging, down to zero, without preloading the inverter, or adding power factor correction filters. In addition, a current-fed inverter, designed to handle power factors down to only 0.7 to 0.8 will not be damaged by power factor transients down to zero. These transients may be of considerable duration; in the order of several minutes. Of most significance is the fact that these power factor transients can be of sufficient duration to start a spin motor, or to permit other typical ac electrical system functions to occur, that may load the inverter with transient power factors beyond its design range. This feature alone makes the current-fed inverter an excellent candidate.

2. The current-fed inverter is inherently free of conducted and radiated EMI

   It is well known that the largest single causes of EMI in a static inverter are sudden changes in the current waveforms within the inverter, as switching occurs. The very nature of the current-fed principle is the prevention of sudden changes in current waveforms in the inverter, and the maintenance of an even level of current flow. This principle, by its very nature, solves a big part of the inverter EMI problem.

The following subsections will discuss, in general terms, the well known and accepted saturated switch-type voltage-fed inverter, and will detail some of its inherent technical failings. The current-fed principle will then be explained and a description presented of how this concept eliminates some of the undesirable circuit limitations of the voltage-fed inverter.

2.1 THE VOLTAGE-FED INVERTER

The voltage-fed inverter circuit is the generally accepted circuit employed in most of today's static inverter designs. A power source is connected through a pair of semiconductor switches, into the ends of a center-tapped transformer primary. For the purposes of our discussion, let us suppose that the power source is a battery, with more than adequate capacity, and with a source impedance so low that it is negligible for discussion purposes. A schematic presentation of the voltage-fed inverter would be as illustrated in Figure 2-1.

When S1 is closed, the full source voltage (minus the semiconductor saturation losses, which we will ignore) will appear across the AB primary of the transformer T1, and conversely, when S2 is closed, the full source voltage will appear across the BC primary.

The switching drive circuit alternately saturates and cuts-off the semiconductor switches, causing an alternating voltage to be generated across the windings of transformer T1, and to be delivered to the load. The power source voltage is directly impressed onto the primary of

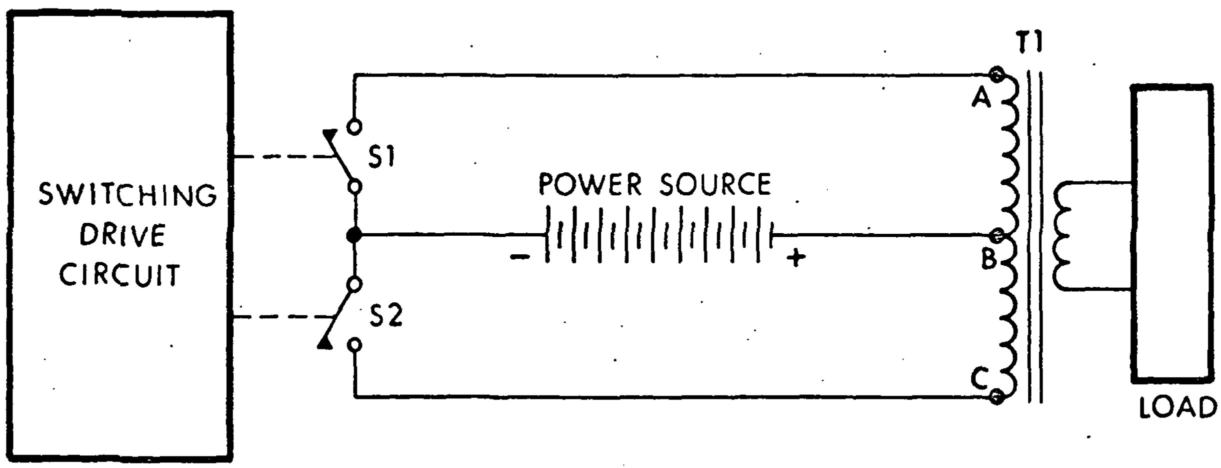


Figure 2-1. Basic Voltage-Fed Inverter Circuit

transformer T1, and therefore, the voltage across the transformer is always a square wave, no matter what the load and no matter how the load power factor varies. The current waveform in the primary of T1 is a different story. It is affected by changes in load, the most important to this discussion, it is affected by changes in power factor.

2.1.1 The Effects of Power Factor

Consider the current waveform in the primary of T1, under various power factor conditions. Also compare the current waveform (in phase relationship), to the voltage impressed by the power source across the primary of T1, when the load is a pure resistive load (power factor 1.0). This comparison reveals waveforms as illustrated in Figure 2-2.

The current waveform will be identical to the voltage waveform. It can be seen that each switch is conducting a full 180 degrees, and the current through the switch, and through the transformer primary, is as high as required to deliver the power demanded by the load. The power delivered by each switch through the transformer primary, is represented by $P = \int EIdt$. When the voltage and current are both in-phase, and square in waveform, then the cross hatched areas in the current waveforms are proportional to the power delivered by each semiconductor switch.

An ac power source that is operating into a power factor load is delivering power to the load, and then receiving power back from the load. This function occurs with each half-cycle. Power is pushed into the load, and then received back from the load. If the ac power source is really a dc source used to operate a static inverter, then the inverter still has to be capable of delivering power to the power factor load, and receiving power back from the load. Any voltage-fed inverter operating into power factor loads uses the principle of holding the voltage fixed (in-phase) relative to the switch conduction time, while the current is forced to shift in phase, and consequently, the current must fluctuate from positive to negative. Because of this, a voltage-fed inverter must have the capability of pushing power into

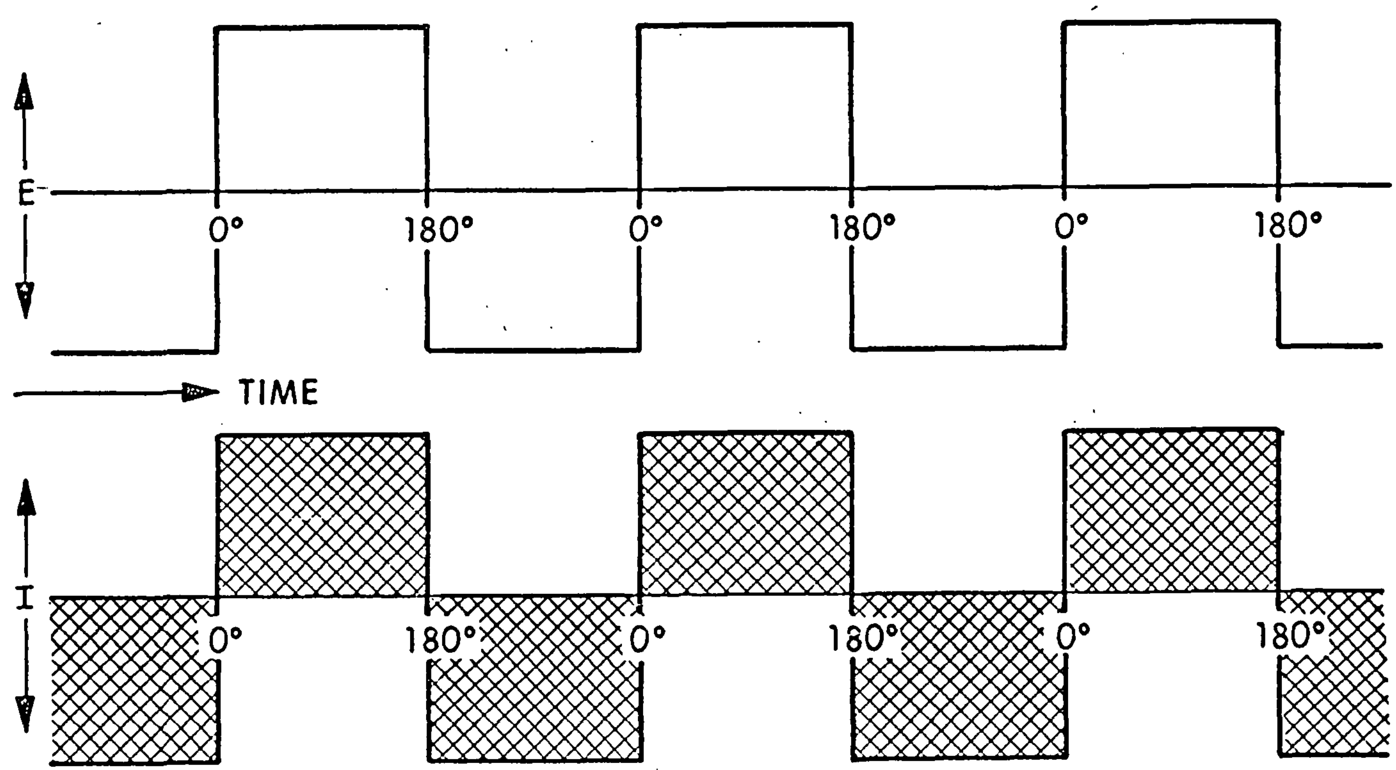


Figure 2-2. Voltage and Current Waveforms for Resistive Load

power factor loads, and then permitting that power to pass back through the inverter into the power source, or it must dissipate the return power on the load side of the inverter.

With the above principle in mind, let us look at an extreme case, with a completely inductive load (power factor zero lagging). When we compare the phase relation of the voltage waveform across the primary of T1, and the current waveform through the primary of T1, this comparison would appear as simplified in Figure 2-3.

When the voltage-fed inverter is faced with the problem of operating into an inductive load, the power that the load attempts to feed back into transformer T1 affects the current waveform in the primary. Semiconductor switch S1 should begin conduction at the 0° conduction angle, but the inductive load is attempting to force a reverse current flow through the switch. Because all semiconductor switches are unidirectional, the switch will block the required reverse current. This interruption of the current flow from the load, when it is at its maximum point, will cause a reverse voltage spike to build up on the primary of T1 and this spike will rise until it exceeds the semiconductor switch rating. In theory, the spike could rise to an infinite voltage, and therefore, the voltage rating of the semiconductor switch is of no consequence. When switch S2 attempts to conduct, at the 180° conduction angle, the same conditions occur.

The energy that the inductive load must feed back into the inverter is represented in Figure 2-3, by the dotted areas in the current waveform. There are only two ways that this energy can be handled. It must either be passed back through the inverter into the power source, or it must be dissipated on the load side of the inverter.

5068

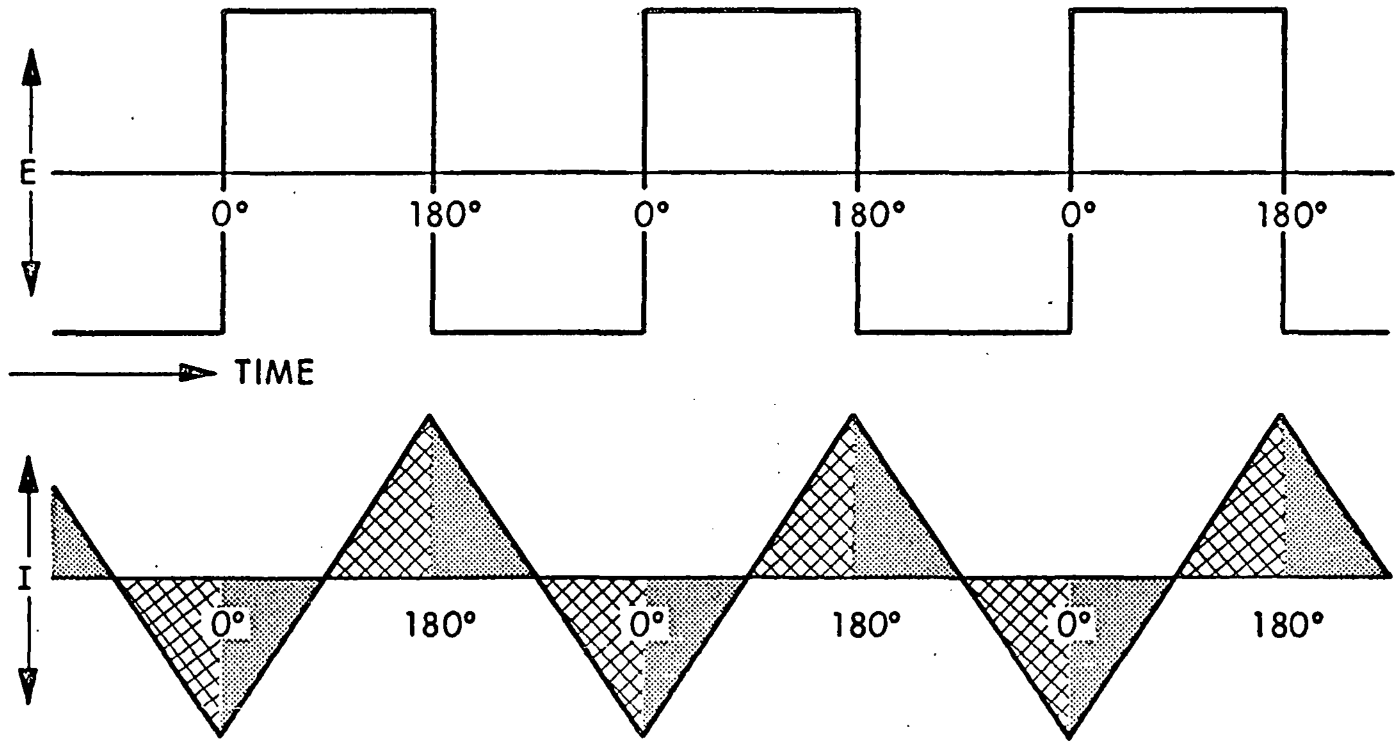


Figure 2-3. Voltage and Current Waveforms for Inductive Load

Dissipating the power that the inductive load must feed back, can be done simply by adding a resistor across the inverter output. In essence, this is pre-loading the inverter, and the pre-load resistor will provide a path for the stored energy in the inductive load.

The load on the inverter therefore appears as an RL load instead of a purely inductive load. Basically, it increases the power factor. This method is very inefficient, and is usually considered acceptable only in very low power inverters.

An alternate consideration would be adding a capacitor to the resistor, and making it an RC network.

A calculation of the losses that will occur in this RC network will show that they are the same as for the pre-load resistor.

Another alternative is to use a back-to-back zener diode arrangement called a de-spiking network. This circuit does exactly the same thing, it dissipates the power feed back from the load.

Another form of pre-load can be accomplished by designing transformer T1 so that it generates considerable internal losses. This will accomplish the same end as the pre-load resistor, and it will incur the same penalty in inverter efficiency, size and weight.

All of these approaches (Ref. Figure 2-4) have one thing in common. They dissipate power that the inductive load must feed back into the inverter. The end result is an inverter with poor efficiency, and an inverter that must deliver much more power than is required by the load alone. The inverter size, weight and cost escalate accordingly.

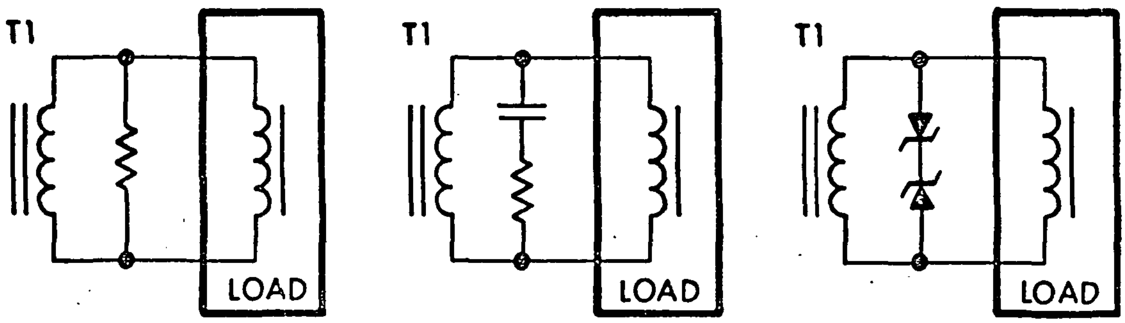


Figure 2-4. Typical Circuits to Dissipate Energy Feed-back from Inductive Loads

35069

Several circuit design methods are used to preserve the energy from the inductive load, and pass it back through the inverter, into the power source. The purpose, of course, is to prevent voltage spikes caused by interrupting the current flow. The basic principle of these circuits is illustrated in Figure 2-5.

An additional secondary winding has been added to transformer T1. Flow of power from the power source through this additional secondary winding is prevented by diodes CR1 and CR2. During operation of the inverter into resistive loads, the number of turns on the additional secondary are adjusted, so that the voltage generated between points D and E is always less than the voltage across the power source.

When the inverter is operating into an inductive load, the energy from the load will cause the same reverse voltage to build up, but as soon as the voltage build-up between points D and E exceeds the power source voltage, the energy will be dumped back into the power source. After the dissipation of energy into the power source has occurred on each half-cycle, the semiconductor switches can begin their conduction. This can be seen in a re-examination of Figure 2-3. The dotted areas in the current waveforms are proportional to the power that the inductive load must feed back, and the cross-hatched areas are proportional to the power that the semiconductor switches must deliver.

Inductive energy dump circuits are all variations on this basic theme. A common variation is to use taps on the primary winding A-B-C (Fig. 2-1) of transformer T1, instead of creating a separate secondary winding.

The most commonly seen solution to handling an inductive power factor with a voltage-fed inverter is simply using a larger inverter to drive a small power factor load. An example could be, using a 500 VA inverter to operate a 100 VA inductive load. This is really a form of preloading the inverter to dissipate the inductive energy that must be fed

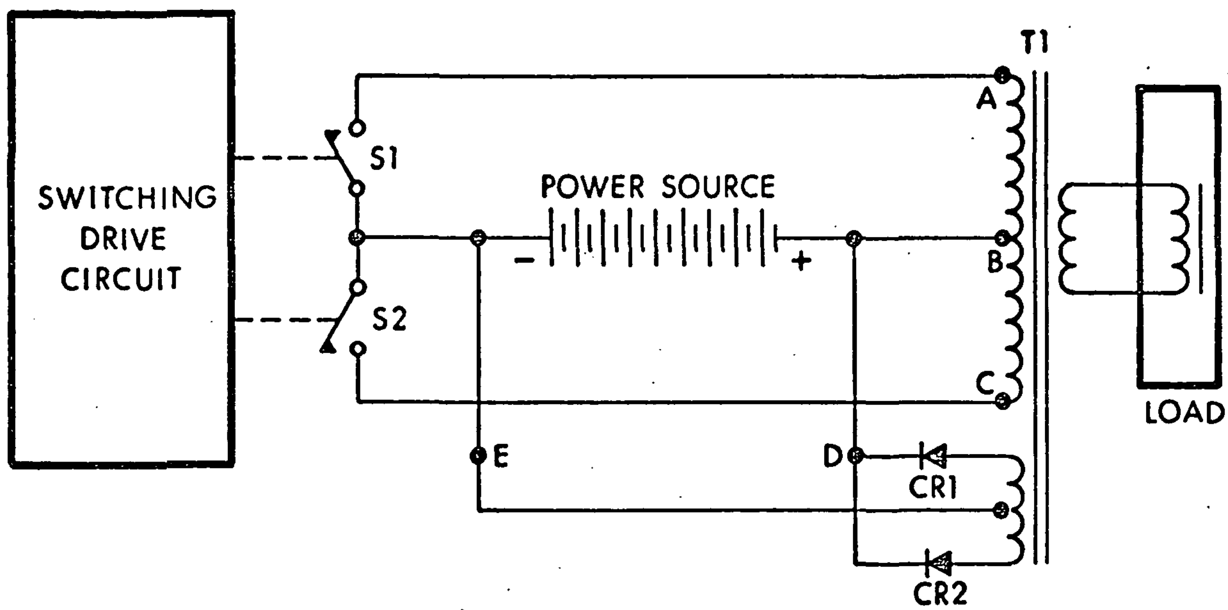


Figure 2-5. Typical Circuit to Transfer Energy from Inductive Loads into the Power Source

5072

back from the load. The preloading, in this case, is simply the internal power loss in the oversized inverter. The inverter, with its larger internal losses, causes the power factor load to become a smaller proportion to the inverter.

The inductive power factor load creates other problems, relative to the utilization of the semiconductor switches. Referencing Figure 2-3, current waveform, consider the time required to discharge the inductive load. Approximately half of the conduction time (from 0 degrees to near 90 degrees) is required, and semiconductor switch S1 could not begin conducting until its allotted conduction time was approximately 50% completed. When conduction begins, the current waveform rises in a quasi-triangular slope as the power is delivered to the inductive load. It can be seen in the Figure 2-3 voltage waveform, that the power source voltage across the primary of transformer T1 retains its square waveform. The power through each switch is presented by $W = \int EIdt$. In Figure 2-3 E is constant and therefore the power delivered by each switch through the transformer primary is proportional to the Idt area cross-hatched under the current waveform triangle.

If the average power delivered by each switch in Figure 2-3 is to be the same as the average power delivered by each switch in Figure 2-2, it becomes apparent that the peak current of the semiconductor switches will have to be much greater, to deliver the same amount of power. Semiconductor switch utilization in the voltage-fed inverter is, therefore, inherently poor when the inverter operates into inductive power factor loads. The current rating of the semiconductors has to be disproportionately large because of this poor utilization. In a voltage-fed inverter, there is no way of improving the switch conduction time, or its conduction current waveform, under inductive load conditions.

There is an additional problem of the utilization of transformer T1. We have established that the semiconductor switches cannot conduct current as desired during 180° conduction time, and therefore, the

peak current through the switch must be correspondingly higher. This means that the peak current through the primary of transformer T1 must be higher. A rough estimation, (based on the simplified diagram illustrated in Figure 2-3) shows, that to obtain the same average current into the primary of T1, the peak current will be four times as great. Therefore, the transformer RMS current would be twice as great, and the wire sizes and construction of the transformer would have to be correspondingly larger.

To illustrate this, the table in Figure 2-6 shows the relationships of peak current to RMS current and to average current, in the transformer.

It is apparent that transformer utilization in the voltage-fed inverter is inherently poor when the inverter operates into inductive power factor loads. The RMS power handling capabilities of the transformer has to be correspondingly large because of this poor utilization. In a voltage-fed inverter there is no way of improving the transformer utilization under inductive power factor loads.

Since the inverter must deliver power into a power factor load, then receive it back, consider effects of a capacitive load on the voltage-fed inverter. At the extreme case, with a completely capacitive load (power factor zero leading) compare the phase relation of the voltage waveform across the primary of T1, and the current waveform through the primary of T1. This comparison would appear as simplified in Figure 2-7.

A capacitive load changes the current waveform through the primary of T1, but the voltage waveform remains unaffected. The voltage waveform remains a square wave, but current spikes now appear in the primary each time the semiconductor switches being to conduct. When the switches begin conducting, they are supplying power in to reverse charge the capacitor, through a very low impedance. With the voltage constant, the current rises to extremely high levels until the capacitor, as it

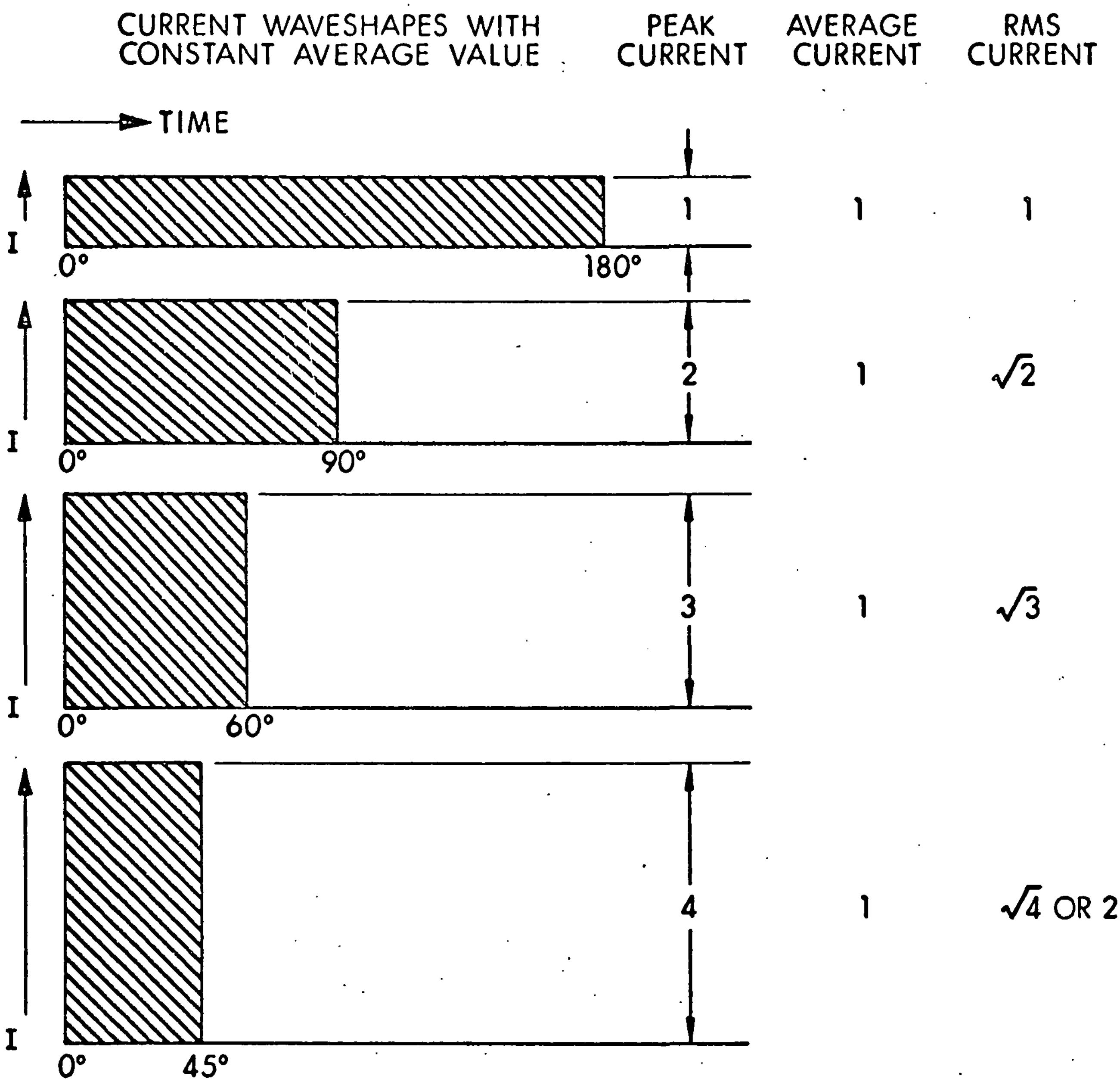


Figure 2-6. Table of Transformer Current Relationships

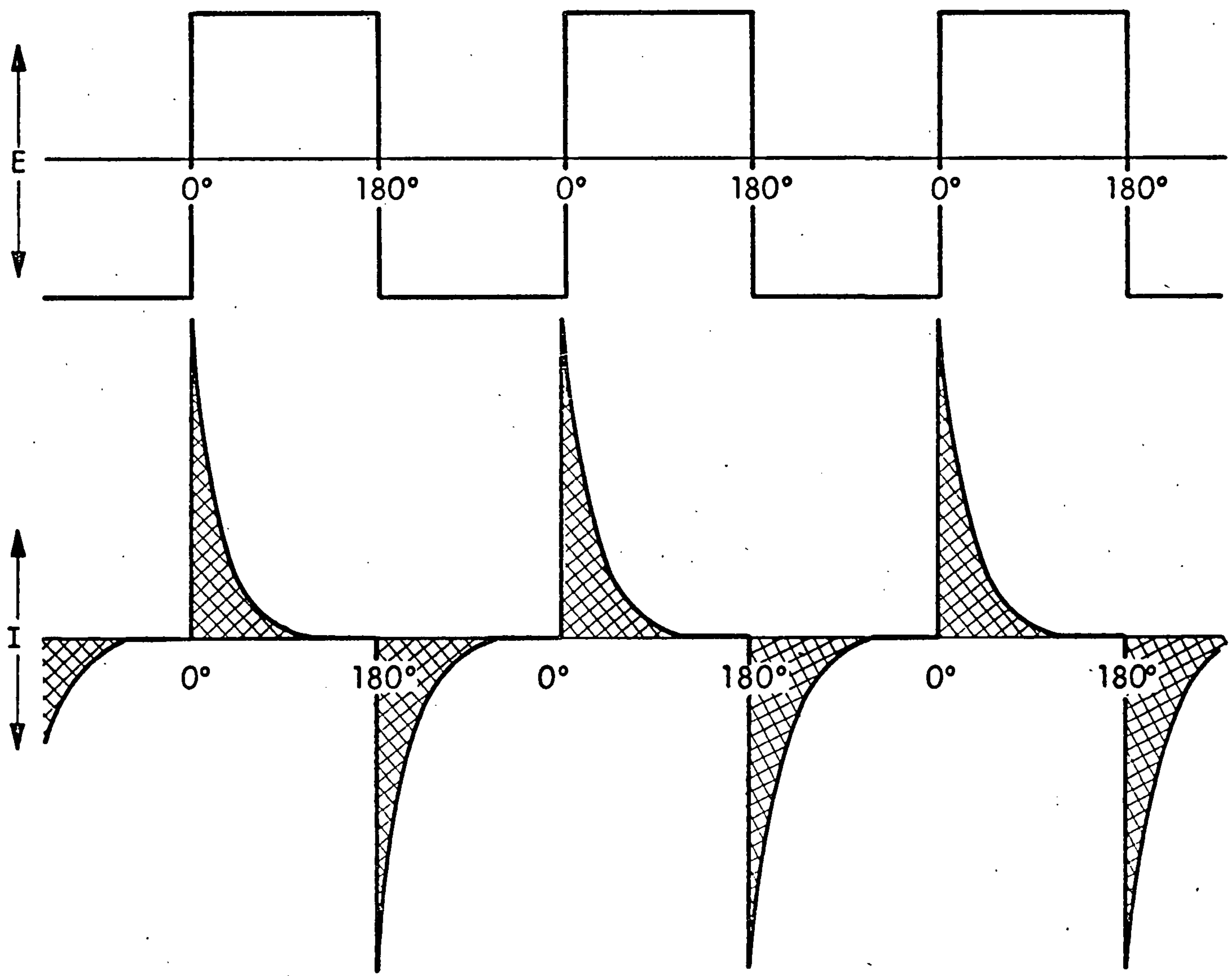


Figure 2-7. Voltage and Current Waveforms for Capacitive Load

charges, begins to represent a rising impedance in the load. Until the capacitor charge rises, there is very little impedance to limit the current inrush, other than the resistance in the transformer wire and the saturation resistance of the semiconductor switches.

Because the current levels can rise to extremely high values as each switch begins to conduct, the I^2R losses in the inverter can rise to very high values, and a consequent reduction in efficiency.

The high peak currents cause transistor switches to exceed the drive power capability, and therefore pull out of saturation into a high-dissipation mode of operation. SCR switches simply generate instantaneous hot-spots due to the extremely high peak currents.

In addition, transformer utilization is decreased because of the high peak currents.

There are no known circuit designs that can be employed by the voltage-fed inverter to enable it to handle capacitive power factor other than the insertion of impedances in the output, to limit the current. Again, the effect on total inverter efficiency, size and weight may result in a very large voltage-fed inverter to drive a very small capacitive load.

The addition of filter in the inverter output to obtain a sine wave will alleviate the capacitive power factor problem to a degree, but it is still a major problem for the voltage-fed inverters. The use of power factor corrective filters will also work, but now the inverter is limited to its operating power factor load point, and cannot operate over a range of power factors.

The principles of power factor operation discussed here are only the basic problems inherent in the voltage-fed inverter design. There are many complicating factors that cause the problems, as discussed, to

become much more complex and difficult to understand. Typical of the complicating factors is the fact that the input power source does not have an infinitely low impedance as assumed in our first statements. Input impedance and input voltage fluctuations may cause additional problems. The inverter seldom operates alone from the battery. Other equipment on the dc input bus restrict the ripple current that the inverter can feed back onto the bus. This forces the use of an LC filter in the input power line.

With the addition of the input filter, we have no reservoir to use for the vital function of pulling power out of, and dumping power back into. To compensate for this, we have to size the capacitor of the LC input filter to a sufficiently large size to permit us to use it as our required reservoir. When we do this, we have the problem of even more complex source impedances.

Losses within the inverter, coupling problems, load changes and other factors all have an impact on the inverter's power factor operation.

The following conclusions were derived from the analysis.

a. It can be designed, within limited range, to operate into inductive loads.

b. It cannot be designed to operate, with high efficiency, into capacitive power factors.

c. Exceeding the power factor design limits even for limited transient periods of time will usually have catastrophic results.

d. It will always be larger, heavier and less efficient when it is designed to operate into power factor loads, than an inverter of the same VA rating operating into purely resistive loads (or than a current-fed inverter of the same VA rating).

2.1.2 Methods of Regulation

Many methods have been developed to provide a means of regulating static inverters. There have been three practical methods evolved from among the many used. These three basic methods of regulation are seen most often in static inverter designs. They are:

a. Pulse-width modulation of the inverter switches.

b. Regulation of the voltage input to the inverter.

c. Use of two inverters in buck-boost mode to supply one output.

It would appear on the first examination, that pulse-width modulation would be the ideal way to achieve regulation in the inverter. This would involve controlling the conduction time of the semiconductor switches, and vary that conduction time to adjust the power delivered by the switches.

Figure 2-8 illustrates the principle. The power delivered by each switch is $W = \int EIdt$. In the case of pulse-width modulation, t becomes the variable that determines the power delivered. An increase in t will deliver more power during each switching cycle, and a decrease in t will deliver less.

The many advantages to pulse-width modulation are obvious. The high power current needs to be handled by only one section (an inverter section), instead of by two sections (a regulator and an inverter section). The total component parts count for a pulse-width modulation regulated inverter can be lower than an inverter regulated by either of the other methods, and the circuitry less complex. These advantages improve reliability and reduce cost.

Figure 2-8 shows that a zero-voltage dwell time occurs between the periods when the semiconductor switches are conducting. This zero voltage dwell time is a period of time when both switches are cut-off and no current is flowing in the primary of transformer T1.

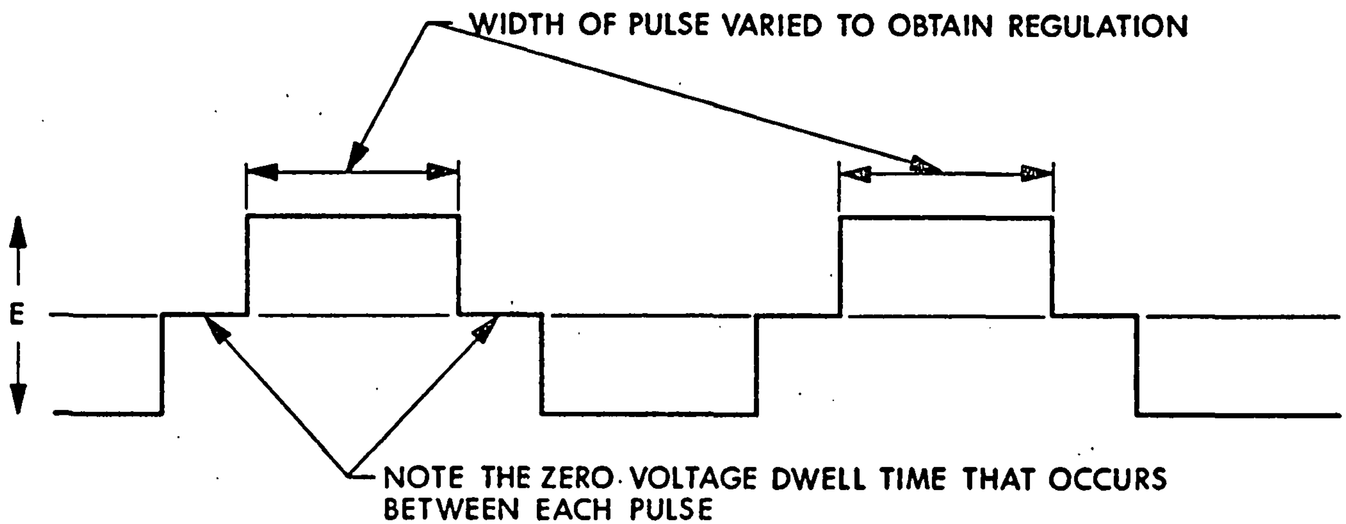


Figure 2-8. Voltage on Primary of T1 when Pulsewidth Modulation is used for Regulation

The circulating currents required by the output filter section are blocked. This single problem has deterred many inverter designers from the use of pulse-width modulation as a method of regulating their inverters.

Most commonly seen as a means of regulating the voltage-fed inverter is the use of a pre-regulator section, that adjusts the voltage into the inverter section to compensate for line and load changes. Sensing is usually done on the inverter output and fed into the regulator section. For very small inverters, a simple dissipative type of series preregulator is sometimes used, but the problem of thermal dissipation and efficiency become too great for this type of regulator to be used on larger inverters.

A high efficiency type of switching regulator is the preference of most inverter designers, who elect to use a pre-regulator. The simplest type of switching pre-regulator is a bucking-type, in which the output voltage is always a volt or two less than the minimum input voltage. Typical state-of-the-art efficiencies for this type of regulator run slightly better than 90 percent. If a buck-boost type of regulator is used, the efficiencies will run slightly lower. This basic regulation method is the most successful regulation method used by the voltage-fed inverter; however, there are still a few problems.

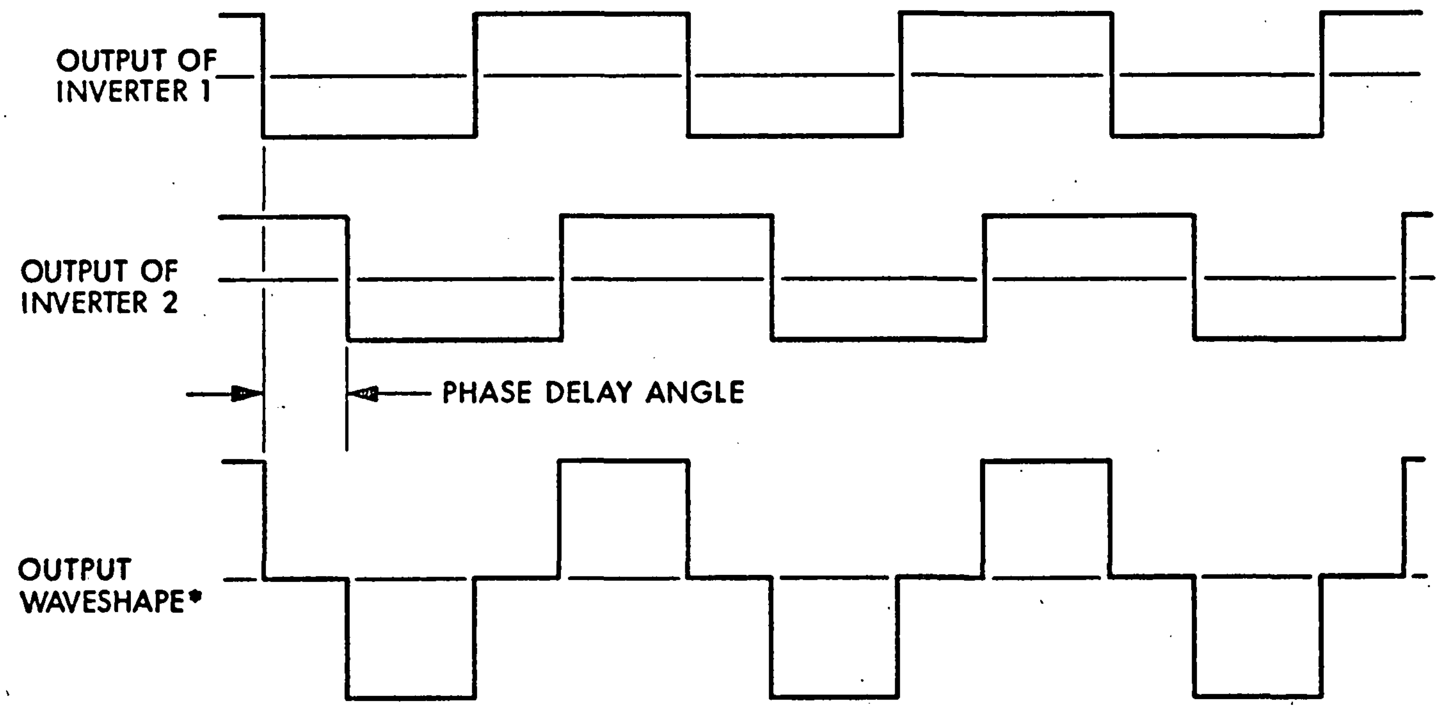
The inverter now has two separate sections, and both are required to handle the main power flow. The power is first regulated by the regulator section, and then converted into ac by the inverter section. The complexity of the inverter plus regulator is increased, and the total component parts count is raised. Subsequent reliability is decreased by this higher parts count. In addition, overall efficiency is affected. For example, if the efficiency of the basic inverter section is 75 percent, the overall efficiency of the total (inverter plus regulator), would be reduced by the pre-regulator efficiency, and the maximum overall efficiency that could be attained would be 67 percent. This decrease in efficiency is caused, of course, by handling the main power stream twice (double conversion) and suffering a compounding of the efficiency figures.

The third method of regulation is the use of two inverters in a buck-boost mode (commonly called a phase shift mode) to supply a single ac output. Figure 2-9 illustrates how this is done.

Inverter No. 1 generates a square wave output, and inverter No. 2 generates another square wave output. When these two inverters are exactly in phase; that is to say, the phase delay angle is 0^{o}, the outputs are directly summed. As soon as a phase delay is added to one inverter, the sum of the two outputs is a semi-square wave, because the square wave outputs of the two inverters will alternately "buck" each other, then "boost" each other, to form the summed output. As the phase delay is increased, the Edt (area)of the semi-square wave is lessened and the output voltage is lowered. When the phase delay is lessened, the output voltage increases. Of course, when the phase angle is shifted a full 180^{o}, the resultant output is zero. This system works well in theory, but in actual operation it creates a problem. One inverter has to deliver power while the other one has to absorb power, a function it cannot do.

In addition, two complete inverters are required for every ac output required. A three phase output, for example, would require six complete inverters. It is obvious how this regulation method causes a sharp increase in the total parts count, with a resultant reduction in reliability. The complexity of the inverter, as well as the size and weight, goes up rapidly.

Reviewing the regulation problem, we see immediately that pulse-width modulation seems to be the most desirable method of regulating an inverter, from the viewpoint of low parts count and lease complexity. This method is seldom used on the voltage-fed inverter because of the technical problems that are involved, but that are not readily apparent. Usually a pre-regulator method of regulation or a phase-shift method of regulation is used on most voltage-fed inverters, at the expense of increased complexity and lowered reliability.



*SUM OF THE TWO INDIVIDUAL INVERTER OUTPUTS

Figure 2-9. Inverter Regulation by Buck-Boost or Phase-Shift Techniques

2.1.3 Motor Starting and Operation

Motor starting and operation is the most difficult load for a voltage-fed static inverter design.

Transformers will always have some slight power factor inherent in their design, but transformers do not correct a power factor. A power factor load on a transformer is simply passed through the transformer to the ac power source. Therefore, a motor load operating from a transformer that obtains its power from a static inverter, will cause the same problems that the motor load would cause if the transformer were not present.

A single inverter driving a single motor is the "worst case" condition for the voltage-fed inverter.

a. There is no way of completely describing a motor load in a specification. It is a non-linear function.

2.1.4 The Voltage-Fed Inverter Problems

a. The voltage-fed inverter can handle inductive power factor only through a limited range. This is because the voltage-fed inverter holds the voltage fixed in phase relative to the switch conduction time, and forces the current to fluctuate from positive to negative under power factor loads. The semiconductor switches, being uni-directional current devices, will not operate in this mode. Auxiliary circuits are necessary to either dissipate the power feed-back from the inductive load, or to by-pass the switches and return the power to the power source.

b. The voltage-fed inverter cannot handle a capacitive power factor. Bleeder resistors to modify the power factor have to be used, or a series impedance in the output is necessary to restrict the current surges.

c. The voltage-fed inverter utilization of the semiconductor switches is poor. The current rating of the switches must be several times larger than necessary to handle the current peaks created by the power factor loads. The high peak currents for short durations is not a desirable condition for the operation of semiconductors, and the reliability of the switches will be degraded.

d. The voltage-fed inverter utilization of the output power transformer is poor. Because of the short conduction time, causing high peak currents required by power factor loads, the transformer will have to be designed for the maximum RMS current, and will be larger and heavier than for resistive loads.

e. The voltage-fed inverter filter circuits will have to be large and heavy. The actual VA circulating in the filter circuits will be large, causing losses and increasing the size and weight of the filter section.

f. Voltage-fed inverters cannot use simple, efficient pulse-width modulation as a means of regulation, because of the transformer problems, and because of the circulating currents required by the filter section. Almost without exception, voltage-fed inverters will use pre-regulators, forcing efficiency down due to double conversion losses, or they will use phase shift, forcing the use of multiple inverters for every output provided.

g. Voltage-fed inverters are never satisfactory when they operate with motors as a load, because current surge required during motor start-up is always coupled with highly inductive power factors, and these conditions change through wide ranges, as the motors come up to speed. The "worst case" condition for a voltage-fed inverter is when a single motor constitutes the only load that the voltage-fed inverter has to drive.

There are two other problems that have not yet been mentioned. These two problems could overshadow all of the other problems discussed to date.

a. The voltage-fed inverter is a high intensity generator of radiated and conducted EMI. This is inherent in the circuit, and there is little that can be done at the EMI source points to reduce the generated radiation levels. Extensive fixes must be incorporated in each different voltage-fed inverter, to reduce these EMI levels. Almost all inverter designs are subject to audio frequency susceptibility problems, and this is discussed in more detail in subsection 2.2.3.

b. The voltage-fed inverter is a generator of considerable audible noise. For example, a voltage-fed inverter with a power output above 1 kW may easily generate sufficient audible noise to cause discomfort to persons close to the inverter. The noise will appear in almost all frequencies in the range of human hearing (above the inverter fundamental) and therefore it is almost impossible to attenuate.

2.2 THE CURRENT-FED INVERTER

In the current-fed inverter circuit, the current is held fixed in phase relative to the switch conduction time, while the voltage is forced to fluctuate from positive to negative. The current-fed inverter performs this, by forcing a constant current flow through the semiconductor switch and through the transformer primary, throughout the entire conduction period of the switch, regardless of the voltage fluctuations. In this manner, the current-fed inverter can deliver power to the power factor load, then receive power back from the load, without passing it back through the inverter.

2.2.1 The Current-Fed Design Concept

A schematic presentation of the current-fed inverter is illustrated in Figure 2-10.

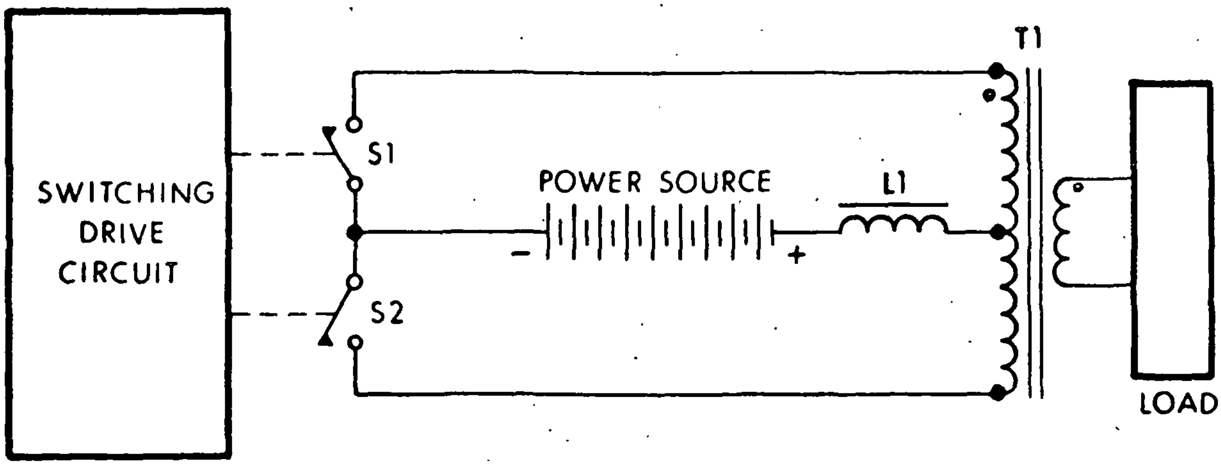


Figure 2-10. Basic Current-Fed Inverter Circuit

Assume that inductor L1 (commonly called the feed-choke) is an inductance of sufficient value to maintain the current flow through the circuit under all conditions. In essence, consider it an infinite inductance. Similar to the operation of the voltage-fed inverter, the switching drive circuit alternately saturates and cuts-off the semiconductor switches. The current flow through the feed-choke, once established, tends to resist any change in current level, and, therefore, different from the voltage-fed inverter, the current through the switches, and through the primary of transformer T1, is maintained as a square wave of constant current value, no matter how the source voltage varies, the load level, or how the load power factor varies.

With this new current-fed inverter concept, we now have a basic circuit than can eliminate many of the problems inherent in the voltage-fed inverter.

The operation of the current-fed square wave inverter circuit depicted in Figure 2-10 can be examined best by comparing the voltage and current waveforms under different conditions.

Under a purely resistive load, the current and voltage waveforms would appear exactly as they do in a voltage-fed inverter, and as illustrated in Figure 2-2. When power factor loads are applied to the current-fed inverter, the voltage waveforms in the output take on a much different appearance. In the voltage-fed inverter, the current waveforms changed.

Under a purely capacitive load (power factor zero leading) or a completely inductive load (power factor zero lagging), the voltage and current waveforms across the primary of the transformer appear as illustrated in Figure 2-11. The waveform of an LCR type of load is also shown.

The feed choke always forces the current in the primary of the transformer to maintain a square waveform, and the voltage now assumes the different waveshapes. The inductive load will cause voltage spikes to appear as indicated in the waveform diagrams, while the capacitive load creates a

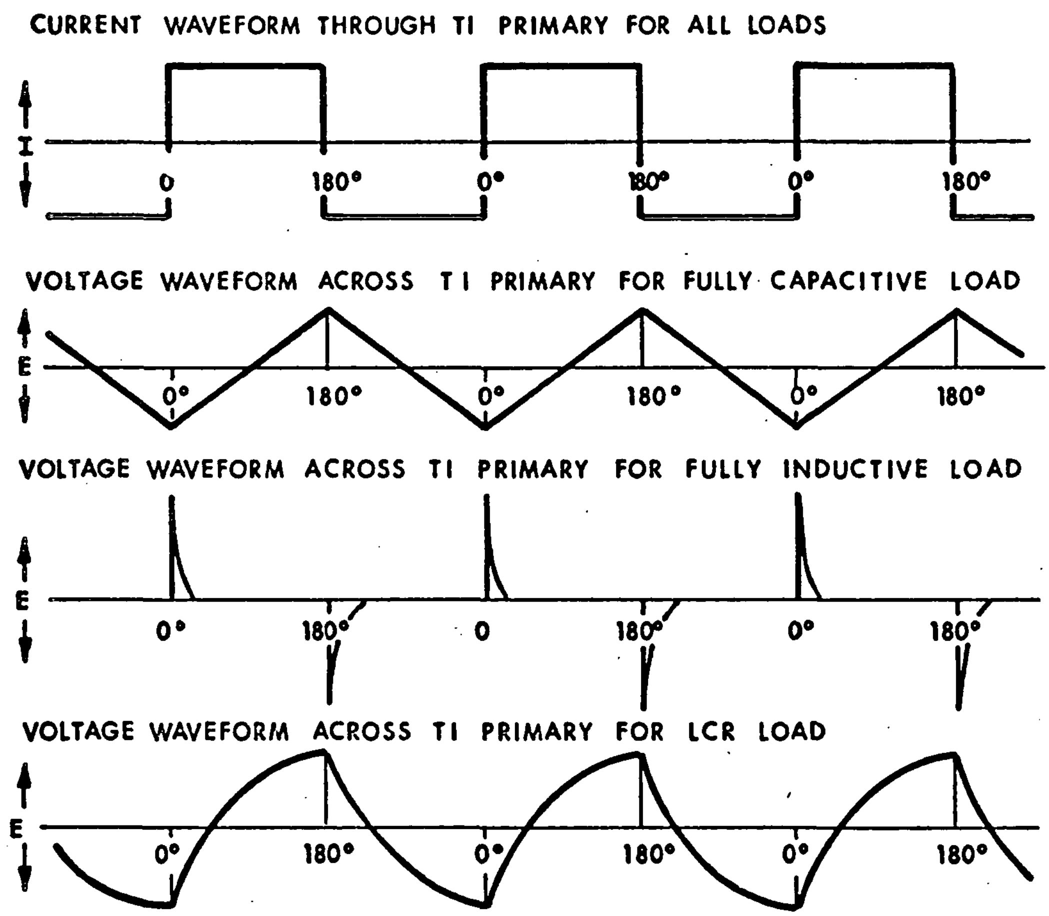


Figure 2-11. Current and Voltage Waveforms for the 2-10 Inverter

triangular voltage waveform. It should be noted that the voltage waveforms in Figure 2-11 are similar to the current waveforms in Figures 2-3 and 2-7.

The voltage waveform for a capacitive load (when compared to the current waveform), shows the capability of handling a power factor. During part of each half cycle, the positive going current waveform remains constant, but the voltage waveform has shifted, and is both positive-going and negative-going during the same half cycle. The source is, therefore, delivering power to the load and then receiving power back from the load during each half cycle without having the power pass back through the inverter. This is the definition of true power factor operation.

If the load is an LCR combination, the voltage waveform would be as illustrated in Figure 2-11. The waveform is part of an e function, rising to approach a finite value. The voltage is both positive-going and negative-going during each half cycle, while the current remains a square wave (forced to remain that way by the feed choke) and the inverter is handling real power factor without having the power pass back through the inverter.

As the combinations of values of the LCR load change, a point is reached where the combination of L and C is resonant at the natural frequency of the inverter. Then the R portion of the load is removed leaving only the resonant L and C combination. The inverter now would appear as illustrated in Figure 2-12.

With the addition of an LC tank circuit in the power output stage, both the voltage and the current waveform out of the tank circuit are sinusoidal. (Ref. Figure 2-13.)

The current waveform through the primary of T1 is a square wave. The feed-choke L1 will force this waveform to be a square wave under any conditions of source voltage waveform or power factor loads. Therefore, the current waveform through the secondary of T1 is also a square wave.

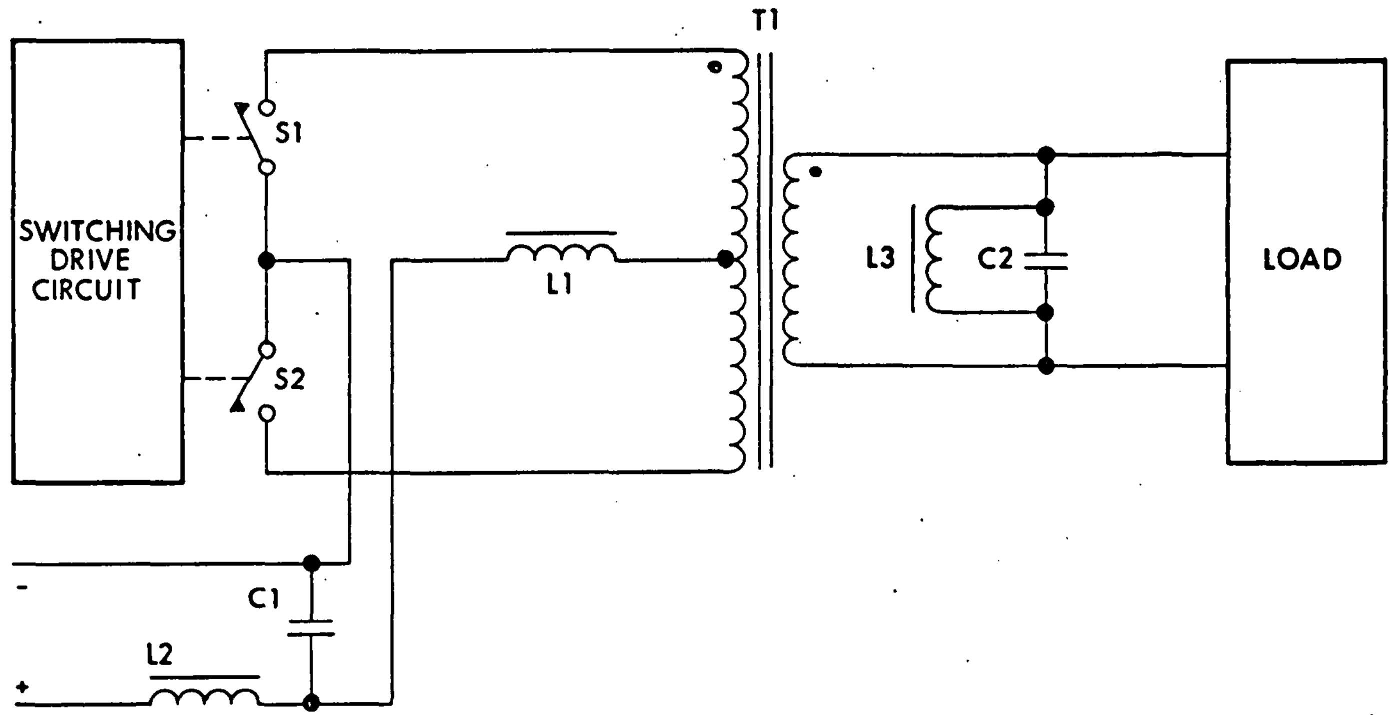


Figure 2-12. Current-Fed Inverter with Natural Sinewave Output

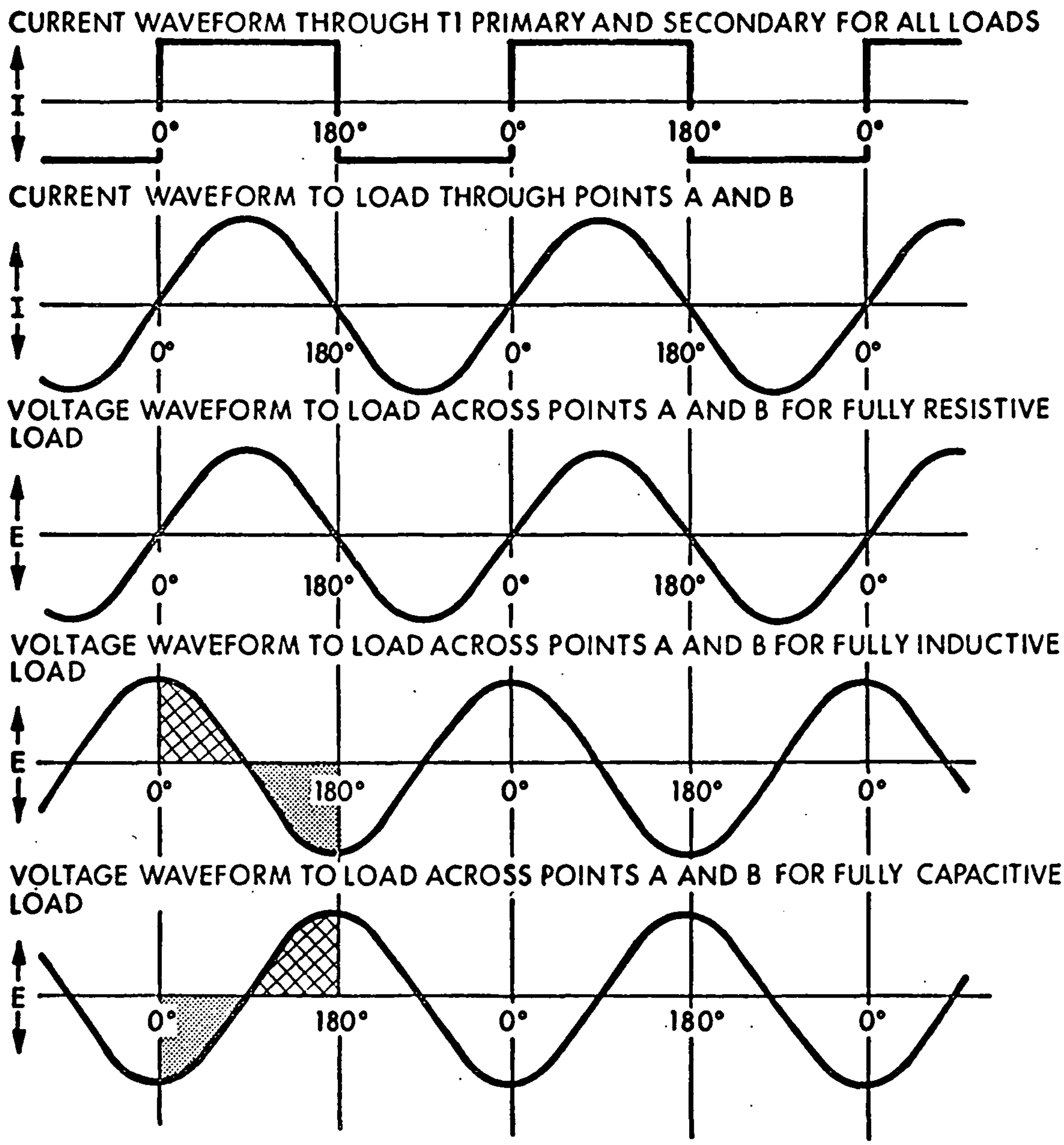


Figure 2-13. Current and Voltage Waveforms for the 2-12 Inverter

35084

The current waveform through points A and B, however, is a sine wave, because of the circulating currents contained in the tank circuit C2-L3. The higher harmonics in the current square wave generated in the secondary of T1 are shunted through C2. The circulating current in the tank is now oscillating between C2 and L3, and theoretically, is not being lost. Only the power demanded by the load is being drawn from this power reservoir in the tank, and the switches have only to supply the difference power lost from the tank into the load.

The tank has added a flywheel effect to the output of the inverter. The circulating currents are maintained in the tank at the natural frequency of the inverter, and the transformer T1 energizes the flywheel each half cycle, and adds only sufficient power to replace the losses from the tank circuit. These losses, in reality, are composed of power delivered to the load, plus small internal losses in the tank.

The power that T1 adds to the tank each half cycle could have any waveform, and the tank will continue to oscillate in a sinusoidal manner. Only the timing of the pulses that energize the tank is critical.

Therefore, the current-fed inverter is handling the power factor, by holding the current fixed, and permitting the voltage waveforms to shift, so that they are both positive-going (cross hatched areas) and negative-going (dotted areas) in the same half-cycle. The inverter is operating into a true power factor load, either capacitive or inductive, without having to pass the power back through the inverter. In addition, it is handling either leading or lagging power factor.

There are several advantages that are realized as a result of incorporating the resonant LC tank into the output circuit. First, the output of the inverter is a natural sine wave, and required no additional filtering. Second, the tank represents a low impedance ac power source to any dynamic load, no matter what the impedance of the dc source that is operating the inverter.

The inductance of L3 can be designed into the secondary of transformer T1, and eliminate L3.

2.2.2 Eliminating the Voltage-Fed Inverter Problems

The current-fed circuit developed to this point has eliminated most of the problems inherent in the voltage-fed circuit.

a. The voltage-fed inverter cannot handle inductive power factor. This problem is not present in the current-fed inverter. The current waveform through points A and B, and to the load, is held exactly in phase by the current square wave pulses generated on the primary of T1. The feed-choke inductor L1 always forces a constant current square wave through the semiconductor switches through the primary of T1. The circulating tank circuit L3 and C2 permits the phase of the voltage at the load to shift, up to a full 90° and the inverter is handling an inductive power factor, (up to zero lagging).

b. The voltage-fed inverter cannot handle capacitive power factor. The current-fed inverter can easily shift the load voltage to a point 90° behind the load current waveform and handle capacitive power factor, (up to zero leading).

c. The voltage-fed inverter utilization of the semiconductor switches is poor. The feed-choke in current-fed inverter forces a constant current through the switches, throughout the entire conduction period, regardless of the voltage on the switch. Utilization of the switch is, therefore, excellent, and the reliability of switches is considerably improved, because the semiconductors are operating in a mode best suited to long life and low stress.

d. The voltage-fed inverter utilization of the transformer is poor. The feed-choke in the current-fed inverter forces a constant current flow through the primary of T1 throughout the entire conduction period of the semiconductor switch, and no current peaks can occur. Therefore, the RMS current through transformer T1 will be at the lowest possible values, and the size and weight of the transformer can be optimized.

e. The voltage-fed inverter filter circuits are large and heavy. The current-fed inverter has no filter section. The output of the inverter is a natural sine wave.

f. The voltage-fed inverter cannot use simple and efficient pulse-width modulation as a means of regulation. Two basic reasons for this were discussed. First, the zero voltage dwell time that occurs between current pulses causes a resetting of transformer T1, and limits the flux density operating range of the transformer. Second, and far more serious, the zero voltage dwell time defeats the normal operation of the filter section. If pulse-width modulation in the current-fed inverter circuit is used as illustrated in Figure 2-12, there is no problem with the transformer utilization, because the tank circuit maintains the voltage on the secondary of T1 as a sine wave, regardless of the current flow through the primary, and re-setting of the transformer during the zero voltage dwell time will not occur. In addition, the current-fed inverter has no filter section, so there is no problem created by the circulating filter currents.

A problem arises, however, if we use pulse-width modulation as the method of regulation. The feed-choke, L1 is forcing a continued current flow, and during the period of time that both semiconductor switches are not conducting, (the zero voltage dwell time), the stored energy in L1 could cause problems. This situation is easily remedied by modifying the feed-choke slightly, as illustrated in Figure 2-14.

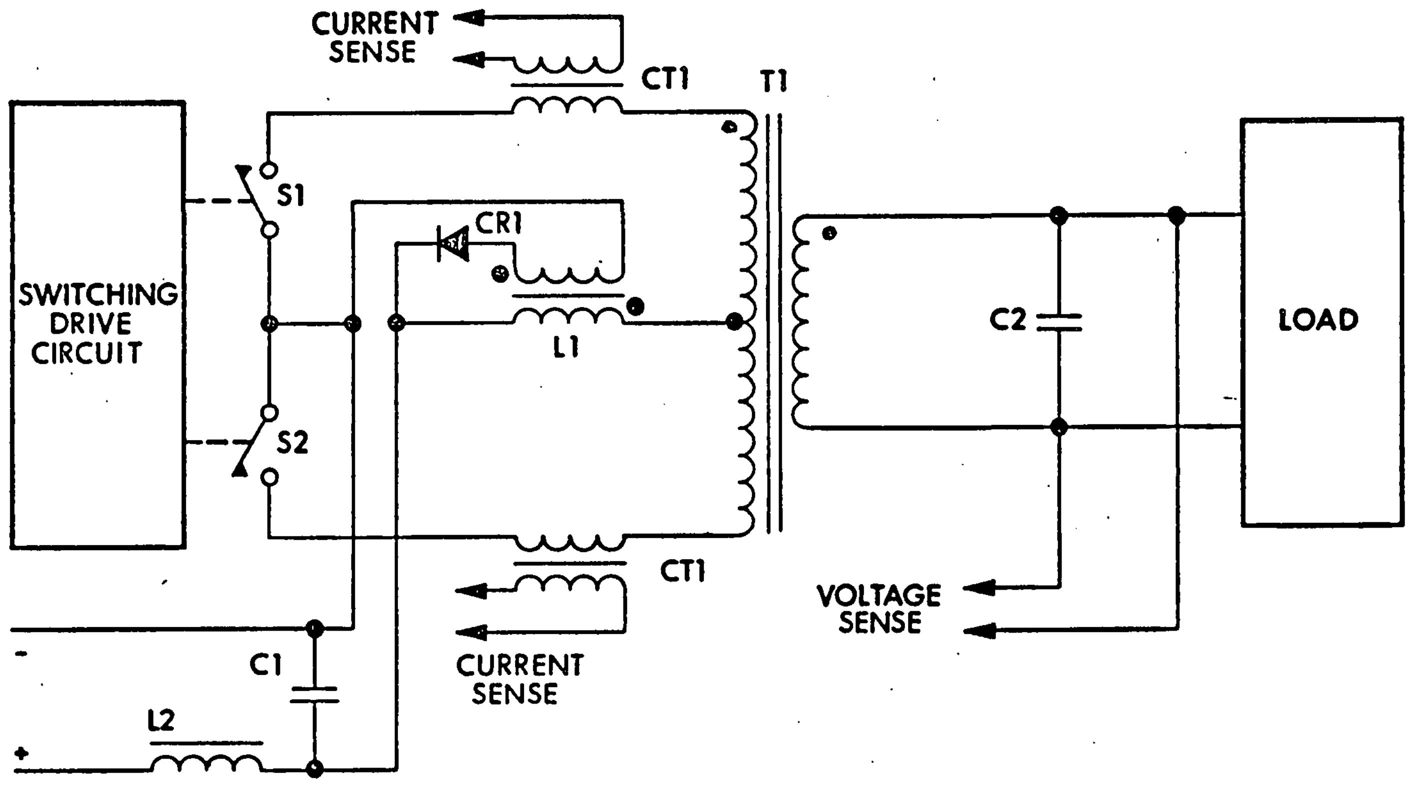


Figure 2-14. Complete Circuit Configuration of Current-Fed Inverter

A secondary winding is added to the feed-choke, and this winding is connected to the power source. A blocking diode CR1 prevents current flow from the power source through the secondary during the normal conduction period of the switches, but when the zero voltage dwell time occurs, then the ampere-turns built up in the primary of the feed-choke are discharged through the secondary.

With the addition of one diode and a secondary winding on the feed-choke, we have enabled the current-fed inverter to use pulse-width modulation as a method of regulation.

g. The voltage-fed inverter is not a satisfactory ac power source for driving motor loads. This is because the motor inrush currents are coupled with the worst-case power factors and these transient conditions change rapidly as the motor comes up to speed.

A plot of the inverter output voltage as a function of the firing angle of the semiconductor switches, is illustrated in Figure 2-15.

The output voltage drops to zero at a firing angle of approximately 60^{o}. This is true for the full design range of input voltage variations. This plot also shows the change in firing angle required to regulate against input voltage variations. In addition, this shows that the inverter will operate into overloads and into a full short circuit condition, by simply shifting the firing angle of the switches to the 60^{o} point. The inverter continues to operate, even though the output is at zero voltage. The inverter has now shifted into a current-limiting mode of operation.

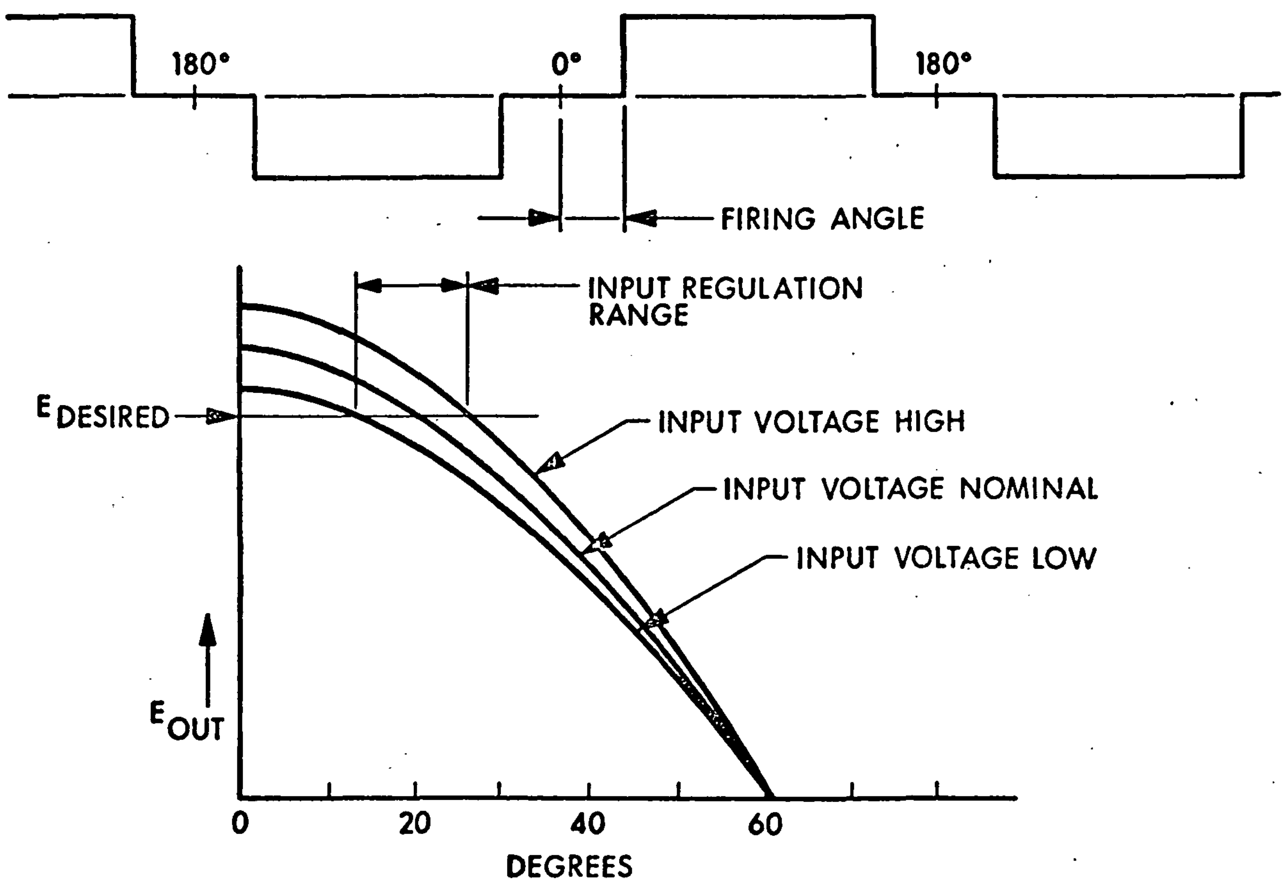


Figure 2-15. Inverter Output as a Function of Firing Angle

Sensing the point at which the current-fed inverter shifts from a voltage regulating mode of operation, now becomes difficult if we sense the output current. The circulating tank provides a reservoir from which surge currents can be drawn, and under power factor loads, the current and the out-of-phase voltage being supplied from the tank are not critical to the operation of the inverter, because they do not represent real power.

The critical element of the output stage is the current through the semiconductor switches. A current sense at this point can provide the necessary signal to shift the inverter from the voltage regulating mode of operation into the current regulating mode. This type of inverter operates with a plot of output voltage versus load as illustrated in Figure 2-16.

In addition, the inverter can withstand sudden power surges coupled with low power factors, as occur when a motor is started. Current transformers CT1 and CT2, in Figure 2-14, illustrate the current sense points.

During motor starting conditions, the inverter overload point is set, so that it shifts into the current limiting mode to handle the motor current inrush. This method of starting the motor will prevent the motor from saturating during starting conditions.

Because the current supplied is constant, full motor starting torque is present, and the motor will come up to speed as fast as if it started from a hard voltage source; however, the heating effects of the saturation currents will be absent, and motor life will be prolonged.

It can easily be seen that the current-fed inverter illustrated in Figure 2-14 operates with motor loads in a manner superior to a hard voltage source. This is because the inverter response loop can be tailored to operate in a stable condition, even with normally unstable histereses motors or other synchronous-type motor.

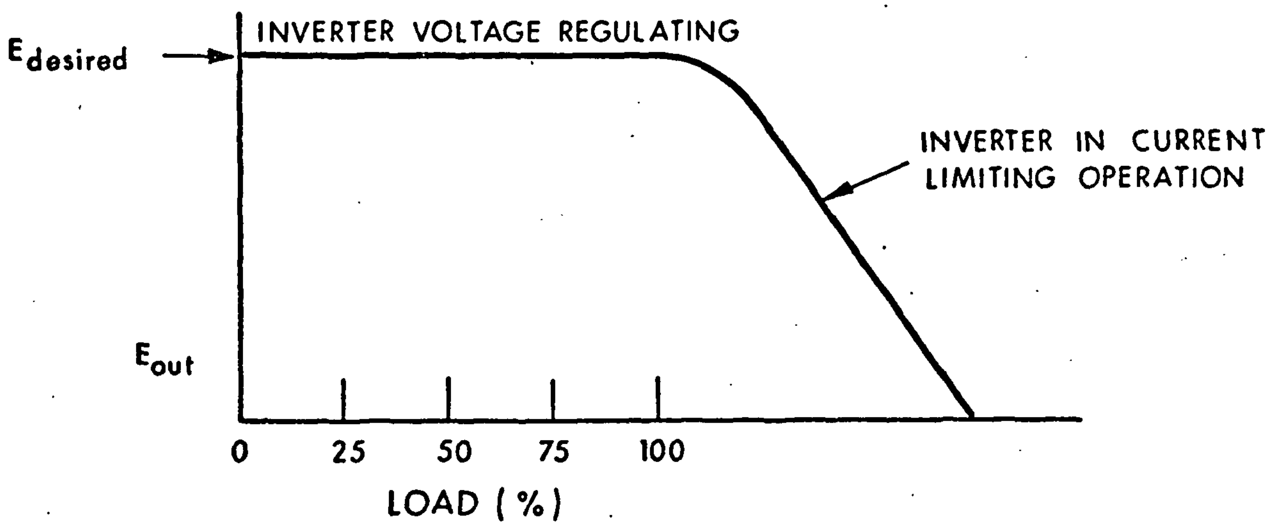


Figure 2-16. Inverter Output as a Function of Load

2.2.3 Conclusions

The preceeding discussion indicated clearly that the current-fed inverter can meet the most important requirement of a partially disabled three phase system to handle leading and lagging power factors. It was also shown that under over-load and even short-circuit condition the current-fed inverter continues to operate and does not need to be "turned on and off" to sense whether or not a short circuit is present.

There is no question that the voltage fed inverter under certain conditions is a good choice. If, however, any power-factor requirements become a necessity the current-fed inverter is best qualified for this application.

In the following discussion let us consider some other technical requirements which result from the goal of having a three phase system remain operative if any one of the three phases fails.

SECTION 3

FEASIBILITY OF A THREE PHASE GENERATION AND DISTRIBUTION SYSTEM

The previous discussion proved that of the two potential approaches only the current-fed inverter can meet the major requirement: Namely in that it can as well meet the power-factor requirement when all three phases are operative as also the additional power-factor requirement imposed by the failure of one phase.

The unique capability of the current-fed inverter to handle any power is based on its operational characteristic to handle power factor by shifting the voltage and keeping the current in phase with the on-time of the semiconductor switches. Therefore, the switches may have to block reverse voltages which they are either inherently capable of or can easily be made capable of doing so through the addition of a diode.

The voltage-fed inverter in a stark contrast keeps the voltage in phase with the on-time of the switches and a power factor causes shifting of the current with the necessity of carrying a negative current under positive voltage conditions. Presently no semiconductor is capable of doing so even if one chooses to put two semiconductors with reversed polarity into a parallel connection. This condition therefore disqualifies the voltage-fed inverter from any inversion application with low power factors.

In the current-fed inverter the current remains in phase with the conduction time of the respective switch. In a single phase inverter it would not have any adverse, if upon application of a power factor the voltage shifts in phase, with respect to the control command of the switches. In a three phase system, however, this does not necessarily apply.

Let us consider a three-phase three channel inverter, where the switches are driven by three squarewave drives which are phased 120° from each

other. With pure resistive load, the voltage remains in phase with the current and the output voltages will also be phased 120° from each other. The same displacement of the voltages remains if the load consists of a balanced power factor load, even though now the voltage is no longer in phase with the switch controls. But as all power factors of the three phases are alike, the voltages maintain their proper phase displacement of 120°. With an unbalanced load, which may be caused by three unequal phase loads or through the loss of one phase, the <u>current</u> phase relation will be maintained at 120° from each other. The <u>voltage</u> displacement of the three phases, however, is no longer maintained at the desired 120° spacing.

The <u>voltage</u> phase relation, however, must be maintained in a three phase system. Therefore, we come to the conclusion that in the current-fed inverter the control pulses to the switches which control the phasing of the current must be controlled in such a manner that the phase voltages maintain their proper relationship.

We notice that in a voltage-fed inverter, where the voltages remain in phase with the switch-control phasing, this requirement is not necessary. But alas a voltage-fed inverter cannot handle the imposed power factors and not at all those caused by the failure of one phase.

It becomes obvious that a control or a compensation circuit is required to keep the voltages of a three phase current-fed inverter in the proper phasing relation to each other.

This requirement certainly presents a technical problem. But solutions to this problem are known and have been proven in numerous Scott-Tee connected three phase current-fed inverters (magnetic amplifiers were used). Also more state of the art circuits are envisioned using integrated circuitry which measure the actual phase displacement and either compensate in the opposite direction or regulate the voltage phase shift by comparing against a reference three phase system. The above mentioned solution

using a magnetic amplifier was extensively used in Scott-Tee three phase connection. It is a relative simple circuit as it uses one phase as the reference- or master-phase.

In this feasibility study we propose a three phase system which will continue to operate as a three phase system after failure of any one phase. This additional condition "failure of any one phase" eliminates the concept of using one phase as the reference- or master-phase as it is unknown which phase might fail. Obviously a different approach is needed which does not rely on one master- or reference-phase.

Figure 3-1 shows a proposed solution: Through the use of integrated circuits a reference three phase square wave system is generated which maintains precise 120^{o} phase displacement between the three reference phases. Figure 3-1 also shows one output sinusoidal phase A which is leading its reference phase by 60^{o}. Generating a synchronized square-wave from the output voltage and comparing it with the reference phase detects a 60^{o} leading phase-shift and causes a 60^{o} lagging base drive for phase A. The end result is that output voltage A is again in phase with reference phase A and proper voltage phasing is maintained.

It becomes apparent that this compensation- or control-circuit for each phase is more complicated than the previously proven phase displacement control. There is, however, no doubt that this technical requirement can be solved efficiently.

The voltage regulating of the phase uses as explained in Section 2 pulse-width modulating of the input voltage. Techniques to accomplish this task are well known, well proven, incorporate self-regenerative drive circuits and do not require further discussions.

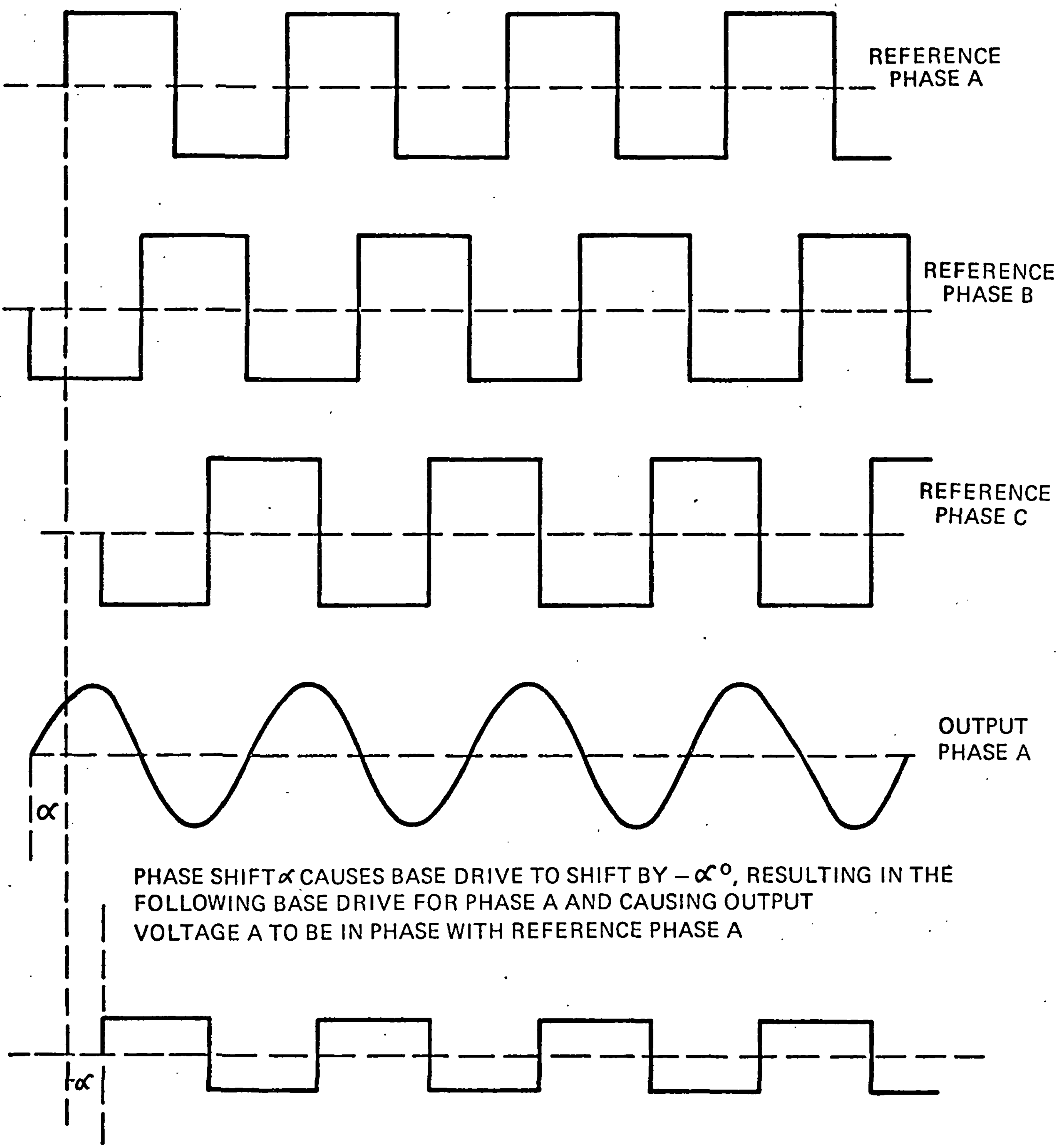


Figure 3-1. Relation Between Reference Phases and Base Drive

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SECTION 4

SPECIFIC DESIGN OF A CURRENT-FED INVERTER

4.1 THE RELATION BETWEEN GENERATED A-C AND D-C INPUT VOLTAGE

For a specific design of a current-fed inverter refer to figure 4-1.

The derivation of the design equations is based on the assumption that the Input Feed-choke L is capable of maintaining a constant current. Even though an infinitely large choke is not feasible the design equations derived under this assumption are more than accurate for any design. Another assumption is that the voltage across the main Inductor-Transformer TI is sinusoidal.

From the preceding discussion it is known that the input current through the switches Ql and Q2 and the two halves of the primary winding on TI are always in phase with the on-time of the switches. If a power factor is imposed the sinusoidal voltage will shift accordingly.

Figure 4-2 shows the current-and voltage-waveshapes across inductor-transformer TI. It is appropriate to use as reference the current-waveshape which remains in phase with the on-time of the switches. The firing angle α, which represents half of the off-time of the switches, counts from the beginning of the DC current-pulses at a conduction time of 180 degrees. The tracing (a) shows the current waveform when a firing angle of α is applied. The conduction time of the current is $180-2\alpha$, the off-time is $2 \cdot \alpha$ and the amplitude of the current is I.

Tracing (b) shows the sinusoidal voltage-waveshape across the terminals 1-2 of inductor-transformer **TI**. The power factor is unity, the phase-shift angle φ is equal to zero and the sine-wave is in phase with the current waveshape.

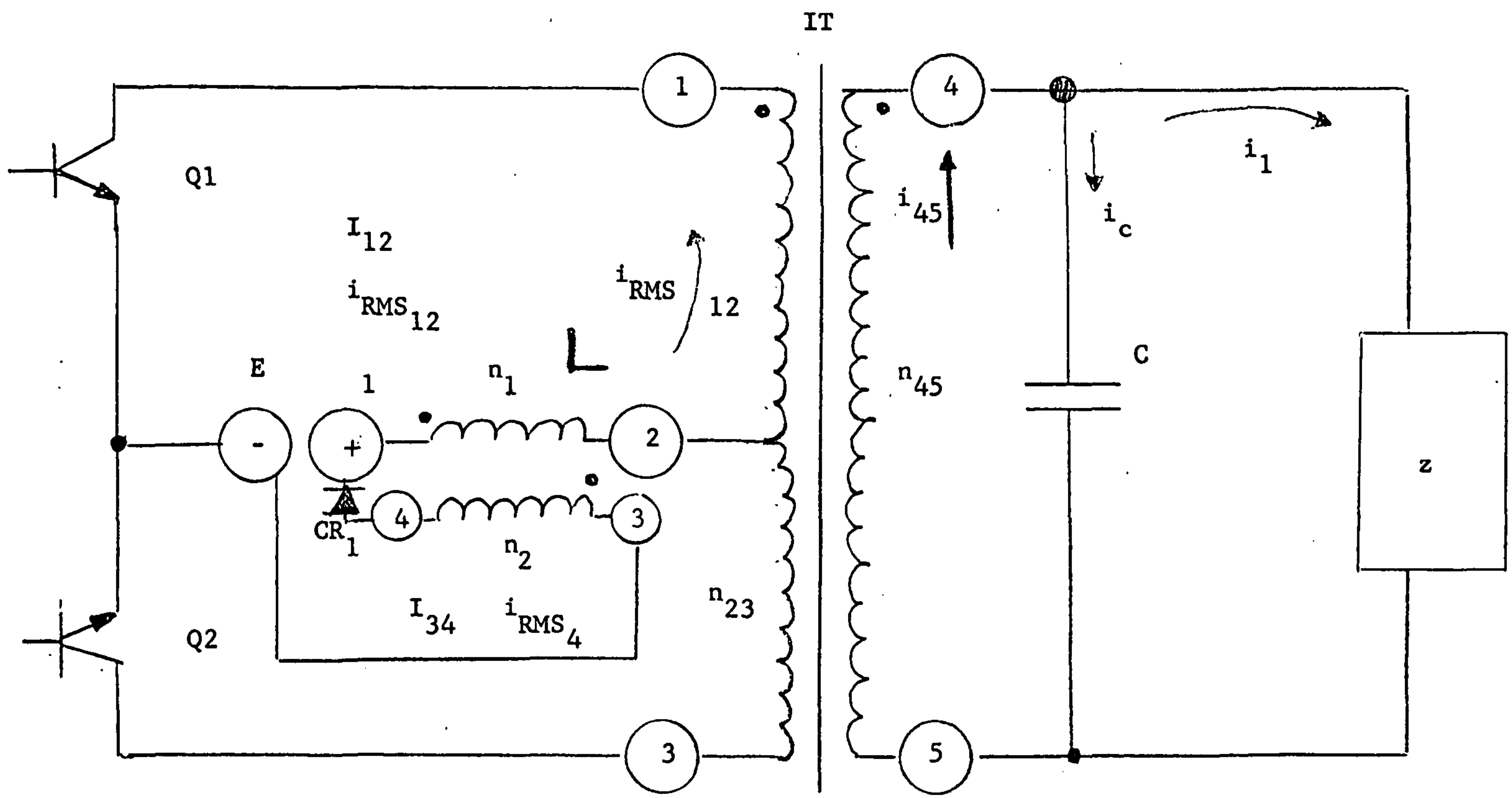
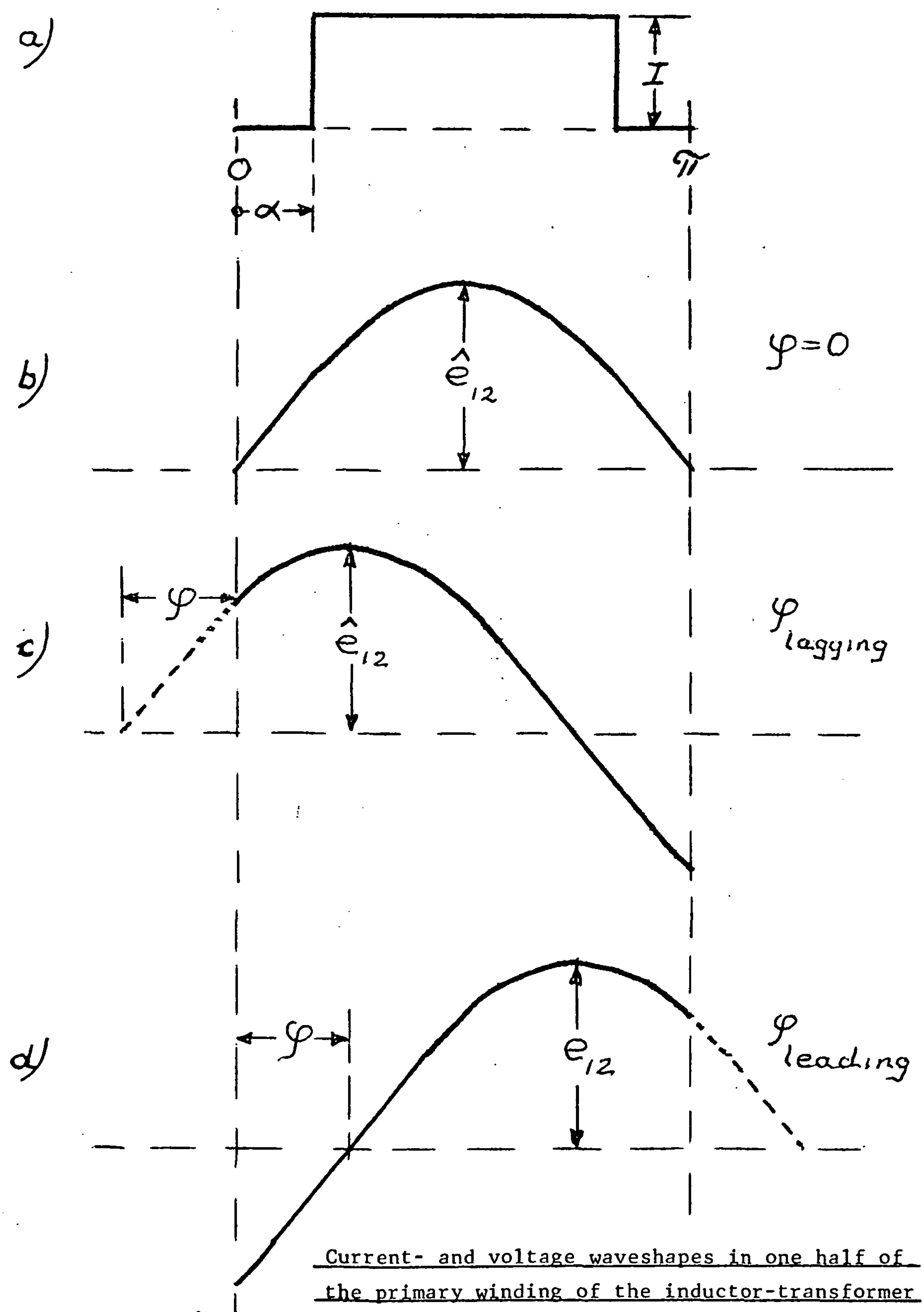


Figure 4-1. Current-Fed Inverter



Current- and voltage waveshapes in one half of the primary winding of the inductor-transformer under varying power factors.

Figure 4-2.

Trace (c) shows the shifting of the sinusoidal voltage under the influence of a lagging power-factor and trace (d) shows the same under the influence of a leading power factor.

The output energy can be calculated for unity, leading and lagging power factors if one uses the limit of the integral as from

$$\alpha \pm \varphi \text{ to } \pi + \alpha \pm \varphi - 2\alpha =$$

$$\alpha \pm \varphi \text{ to } \pi - (\alpha \mp \varphi)$$

The integral for the output energy W_{out} is then:

$$(1) \quad W_{out} = \int_{\alpha \pm \varphi}^{\pi - (\alpha \mp \varphi)} (I\, \hat{e}_{12} \sin x)\, dx = I\, e_{12} \left[-\cos x \right]_{\alpha \mp \varphi}^{\pi - (\alpha \mp \varphi)}$$

$$= -I\, \hat{e}_{12} \left[\cos(\pi - \langle \alpha \mp \varphi \rangle) - \cos(\alpha \pm \varphi) \right]$$

$$= -I\, \hat{e}_{12} \left[-\cos(\alpha \mp \varphi) - \cos(\alpha \pm \varphi) \right]$$

$$= I\, \hat{e}_{12} \left[\cos(\alpha \mp \varphi) + \cos(\alpha \pm \varphi) \right]$$

$$= I\, \hat{e}_{12} \left[\cos\alpha \cdot \cos\varphi + \sin\alpha \cdot \sin\varphi + \cos\alpha \cdot \cos\varphi - \sin\alpha \cdot \sin\varphi \right]$$

$$(2) \quad W_{out} = 2\, I\, \hat{e}_{12} (\cos\alpha \cdot \cos\varphi)$$

The input energy is delivered to the load during the on-time $(\pi - 2\alpha)$ of the switches and energy is fed back into the input source by the secondary of the feed-choke L which has the turns ratio $n_1 : n_2$.

The input energy is:

$$(-3) \quad W_{in} = EI \; (\pi - 2\alpha) \; - EI \frac{n_1}{n_2} \; -2\alpha$$

$$= EI \; (\pi - 2\alpha - \frac{n_1}{n_2} \; 2\alpha)$$

$$(-4) \quad W_{in} = EI \left[\pi - 2\alpha \left\langle 1 + \frac{n_1}{n_2} \right\rangle \right]$$

Under the assumption of no losses, the input energy equals the output energy. Equating (-2) and (-4) yields

$$\boxed{(-5) \quad e_{12} = E \times \frac{\pi - 2\alpha \left(1 + \frac{n_1}{n_2}\right)}{\sqrt{2} \; 2 \quad \cos \alpha \times \cos \varphi}}$$

where e_{12} . . . . RMS value of AC voltage across one half of primary of TI

E . . . . . DC input voltage

α . . . . . firing angle in radians (= 1/2 of off time)

$n_1 : n_2$ . . . turns ratio of feed choke L

$\cos \varphi$ . . . leading or lagging power factor of load

It is important to note that at a fixed DC input voltage E the generated AC voltage is not only a function of the firing angle α (or the conductance time $180-2\alpha$) but also a function of the turns ratio $n_1 : n_2$ of the feed-choke L and the power factor $\cos \varphi$ of the load. Leading <u>and</u> lagging power factors have the same influence.

It is further noteworthy that the AC voltage becomes equal to zero when $\pi = 2\alpha\left(1 + \frac{n_1}{n_2}\right)$. This fact allows for keeping the inverter running, generate zero AC output voltage and hence have a short-circuit proof design. This capability of delivering a short-circuit current of equal or greater magnitude than the nominal output current and yet at a regulated value is advantageous in starting up motors. An in-rush current, which in squirrel cage or other induction motors is 5 to 7 times the nominal current is always avoided and yet the motor starts up with the maximum torque.

Whenever the danger of an in-rush current may be damaging either to the inverter or to the load this type of short circuit protection is more suitable than the often used "on-off-on-off" approach.

Past experience has shown that a turns ratio of $n_1 : n_2 = 1:2$ on the feed-choke yields the best compromise between the imposed blocking voltages on the switches, the optimum design of the feed-choke and the available range of conduction angle.

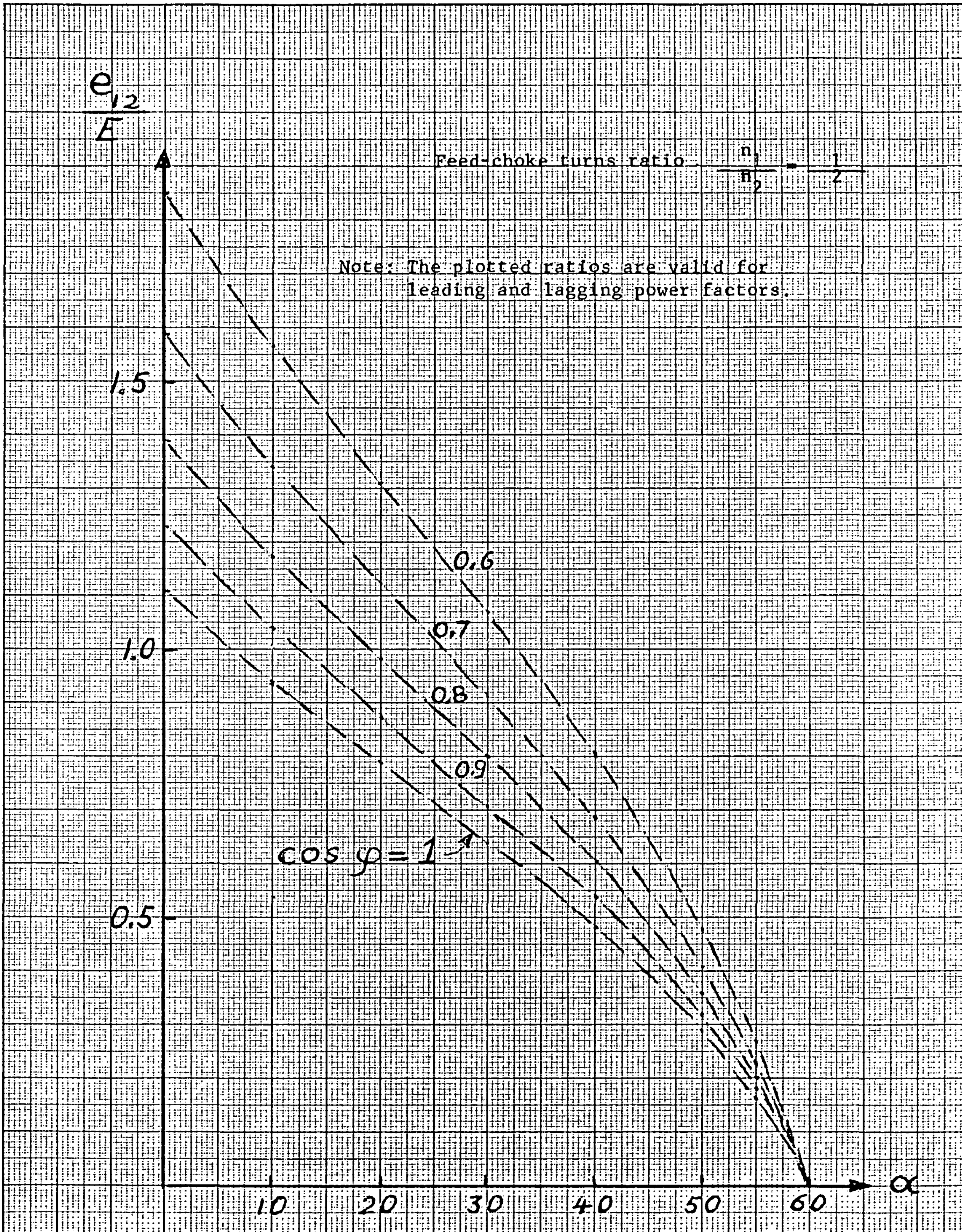
Figure 4-3 shows at a feed-choke turns ratio $n_1 : n_2 = 1:2$ the ratio of $\frac{e_{12}}{E}$ as function of firing angle α and power factor factor $\cos \varphi$.

4.2 THE RMS CURRENT THROUGH EACH HALF OF THE PRIMARY WINDING ON INDUCTOR-TRANSFORMER TI

Each half of the primary winding on inductor transformer TI carries every other half cycle a current of rectangular waveshape. The amplitude is I and the length is $(\pi - 2\alpha)$ (where α is expressed in radians). The RMS value of this current which is the determining value in selecting the wire size is

$$(-6) \qquad i_{RMS_{12}} = I \sqrt{\frac{\pi - 2\alpha}{2\pi}}$$

The voltage waveshape e_{12} is, as stated before, of sinusoidal waveshape.



Ratio of e_{12}/E as function of firing angle α and power factor $\cos \varphi$

Figure 4-3

4.3 THE SECONDARY RMS CURRENT ON INDUCTOR-TRANSFORMER TI

The secondary current on inductor-transformer TI consists of the resonant capacitive current through capacitor C and the output current. The latter may be resistive or may be governed by the power factor of the load. (Refer to figure 4-1). As the output e_{out} is sinusoidal all currents can be added vectorially. The RMS current $i_{RMS_{45}}$ through the secondary winding is therefore

$$i_{RMS_{45}} = \vec{i}_C + \vec{i}_L$$

$$i^2_{RMS_{45}} = i^2_C + i^2_{out} - 2\, i_c i_{out} \times \cos\,(90 \pm \varphi)$$

$$= i^2_c + i^2_{out} - 2\, i_c i_{out}\ (\mp \sin 90 \sin \varphi)$$

(-7) $$i_{RMS_{45}} = \sqrt{i^2_c + i^2_{out} \pm 2\, i_c i_{out} \sin \varphi}$$

where $i_c = e_{out}\ \omega C$

$i_{out} = e_{out} / Z$ where $Z = \sqrt{R^2 + X^2}$

4.4 THE VA_{RMS} RATING OF INDUCTOR-TRANSFORMER TI

For the circuit configuration as shown in figure 4-1 the total VA_{RMS} rating of the inductor transformer is then:

(-8) $$VA_{RMS_{TI}} = 2\, e_{12} \times i_{RMS_{12}} + e_{out} \times i_{RMS_{45}}$$

4.5 THE SELECTION OF THE INDUCTANCE OF TI AND OF THE VALUE OF CAPACITOR C

The main criterion for the selection of the capacitance value of C is the acceptable harmonic content or distortion of the output waveshape. Once the value of the capacitor C is known the inductance value of the winding on TI across which the capacitor is connected can be calculated as the resonant value at the operating frequency.

The input power is delivered in DC current-pulses of rectangular waveshape. The amplitude is I and the maximum duration is one half cycle.

Based on Fourier Analysis a rectangular waveshape has the highest harmonic content when its duration is one half cycle. This then represents the worst case. If we assign to the fundamental the value of 100 percent then the following higher harmonics are present in the following percentages:

Harmonic	1st	3rd	5th	7th	9th	11th
Content in %	100	33.3	20	14.3	11.1	9.09

Any load having a series connected reactive component represents the lowest impedance as function of frequency at a power factor of unity. In this case the lowest impedance value is equal to the resistive value.

The fundamental component of the rectangular waveshape encounters a (theoretically) infinite impedance in the parallel resonant circuit and hence appears in full across the load. All higher harmonics will be divided between the capacitor and the load in accordance to their respective impedances. If for instance the impedance of the capacitor at the fundamental frequency is equal to the load resistor R, then the third harmonic will encounter the load resistor at its full value, the capacitor however only at one third of the same value. The ripple current through the capacitor will be three times higher than through the load resistor.

Approximately 25 percent of the third harmonic flows through the load resistor and 75 percent through capacitor C. The figures are approximate only but close because the harmonic's voltage phase relation is neglected. To be on the safe side it is commonly assumed that the third harmonic is reduced by a factor of three, the fifth harmonic by a factor of five, etc., and this holds true when at the fundamental frequency R was equal to $\frac{1}{\omega c}$. If the ratio of R:$\frac{1}{\omega c}$ is greater than unity an accordingly large reduction in harmonic distortion takes place.

The following tabulation shows the harmonic content or distortion in percent as function of the ratio R over $\frac{1}{\omega c}$:

$\frac{R}{\frac{1}{\omega c}}$	Number of Harmonic 1	3	5	7	9	11	Approximate Total Distortion in Percent
1	100	11.111	4.000	2.041	1.235	0.826	12.1
2	100	5.556	2.000	1.020	0.617	0.413	6.04
3	100	3.703	1.333	0.680	0.411	0.275	4.02
4	100	2.778	1.000	0.510	0.309	0.207	3.02

As the tabulation shows the major distortion is caused by the third harmonic. It is therefore common practice to select a ratio of $\frac{R}{\frac{1}{\omega c}} = 2$, avoid a large resonant circuit and if necessary remove the third harmonic through the use of a specially tuned third harmonic series resonant circuit.

As a general rule we can therefore state:

$$C_{res} \approx \frac{2}{\omega R_{load_{min.}}} \tag{-9}$$

where

C_{res} . . . . resonant capacitance

ω . . . . . frequency of inverter

$R_{load_{min}}$ ... minimum load resistance

Note: C_{res} and R_{load} are always referred to the same voltage or winding.

The value of the inductance of the winding on inductor-transformer TI is then readily determined from the resonance equation

$$\text{(-10)} \qquad L_{res} = \frac{1}{\omega^2 C_{res}}$$

4.6 THE SELECTION OF THE FEED-CHOKE L.

For the design of the feed-choke L two parameters need to be selected first. These parameters are:

a. Turns ratio $n_1:n_2$ of primary winding to secondary winding.

b. Inductance of primary winding.

a. The selection of the turns ratio $n_1:n_2$ of the feed choke L is governed by equation (-5) . The following tabulation shows the range of the firing angle α and the range of the conduction angle $180-2\alpha$ as function of the feed choke's turns ratio $n_1:n_2$:

$n_1:n_2$	Firing Angle α	Conduction Angle $180-2\alpha$
1:1	0 to 45^o	180 to 90^o
1:2	0 to 60^o	180 to 60^o
1:3	0 to 67.5^o	180 to 45^o
1:4	0 to 72^o	180 to 36^o
1:5	0 to 75^o	180 to 30^o

It should be noted however that a change of turns-ratio not only affects firing-and conduction-angle but also the RMS values of the currents and the blocking voltage imposed on the switches. A turns ratio of $n_1:n_2 = 1:5$ for instance adds to the sinusoidal blocking voltage an induced voltage of five times the input voltage.

For these reasons the most commonly selected turns ratio $n_1:n_2$ for the feed choke is:

(-11) $$n_1:n_2 = 1:2$$

b. The selection of the minimum primary inductance of the feed-choke L is based on two criteria.

The first criterion requires that the feed-choke be capable of operating over the full control range and should therefore be capable of absorbing the AC voltage which occurs when the firing angle α and the input voltage E become maximum and the AC output voltage of the inverter becomes zero. During the on-time of the switches the full DC voltage is absorbed by the primary of the feed-choke and during the off time the secondary winding feeds the stored energy back into the DC source.

The primary of the feed-choke must therefore be capable of absorbing the following volt-seconds without saturating and proper selection of the maximum flux density is possible:

$$\mathrm{edt}_{L_{prim}} = \frac{1}{2} E_{max} \left(1 - \frac{1}{1 + \frac{n_1}{n_2}} \right) T$$

(-12)

$$\mathrm{edt}_{L_{prim}} = \frac{E_{max}}{2f} \left(1 - \frac{1}{1 + \frac{n_1}{n_2}} \right) \quad \left[\text{Volt-seconds}\right]$$

where E_{max} . . . . max DC input voltage

f. . . . . . operating frequency in Hz

$n_1:n_2$. . . . turns ratio of feed choke

The second criterion must assure an uninterrupted current flow in the feed-choke. This condition must be fulfilled at minimum loading (or maximum load resistor) and with the maximum AC voltage across the inductor L. At a conduction angle of 180 degrees the full AC component of the rectified AC voltage of one half of the primary of the inductor-transformer appears across the primary of the feed-choke L. If we refer the maximum load resistance $R_{12_{max}}$ (minimum loading) to one half of the primary then the minimum required primary inductance of the feed-choke is

$$L_{12_{min}} = \frac{0.06 \times R_{12_{max}}}{f} \quad [H] \tag{-13}$$

where f . . . . .operating frequency in Hz

The above equation can be derived as shown in the appendix.

Three more parameters are required for the design of the feed-choke L:

After the firing angle α and the conduction angle $(180-2\alpha)$ have been determined through the use of equation (-5) the amplitude of the DC current I can be calculated through the use of equation (-4) . Some allowance should be made for the expected losses and the input power adjusted accordingly.

With the knowledge of the values of I and α the RMS currents through primary and secondary winding of the feed-choke can be calculated.

They are:

$$(-14) \qquad i_{RMS_{L_{n_{12}}}} = I \sqrt{\frac{\pi - 2\alpha}{\pi}}$$

where α in radians

and

$$(-15.) \qquad i_{RMS_{L_{n_{34}}}} = I \frac{n_1}{n_2} \sqrt{\frac{2\alpha}{\pi}}$$

SECTION 5

THE CIRCUIT OF THE CURRENT-FED INVERTER

The complete circuit diagram of the operating breadboard of the current-fed inverter is shown in figure 5-1.

To ease explanation of operation the complete circuit diagram is broken down into the following eight subcircuits:

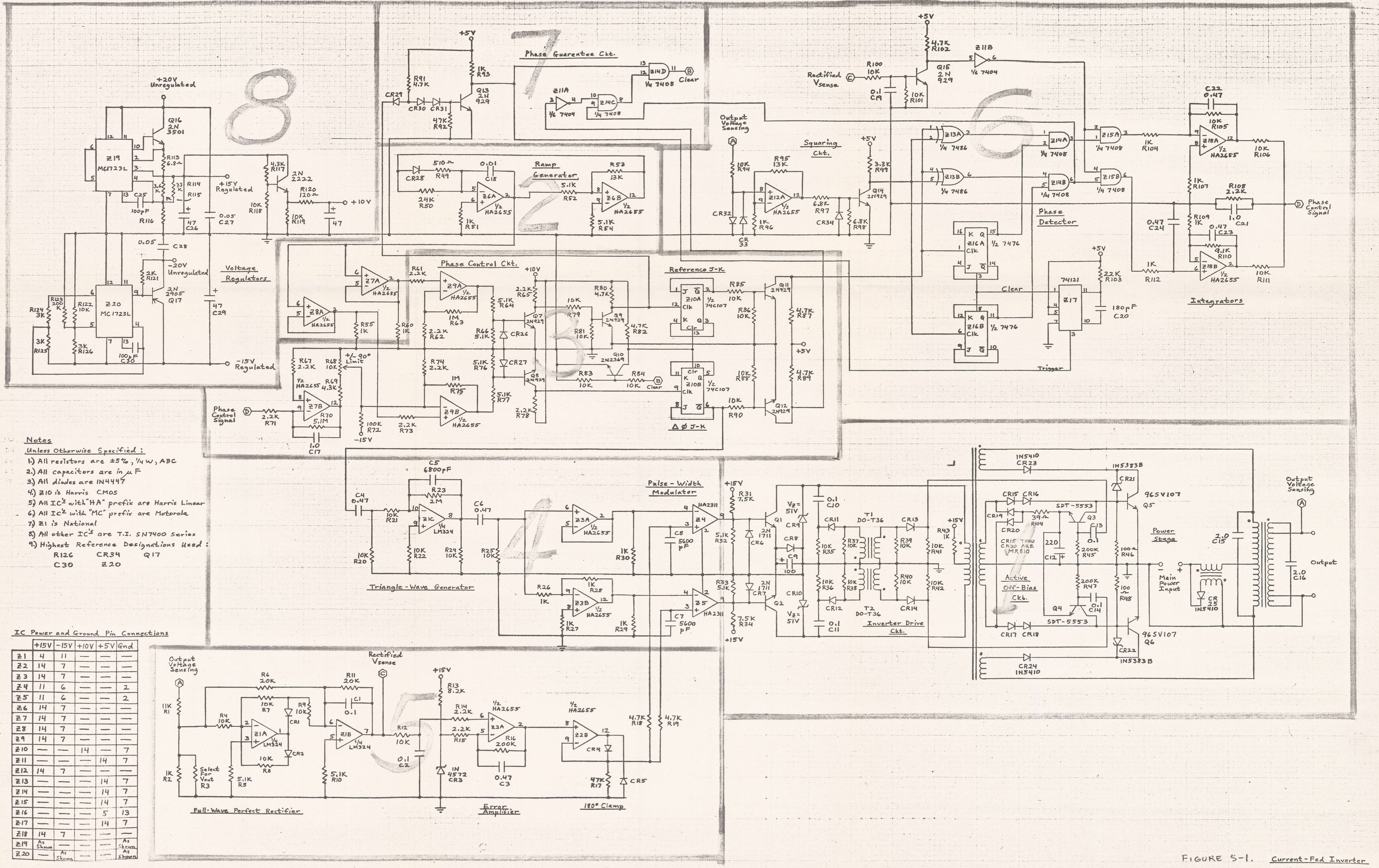
1. Power stage driver stage and active off bias circuit.
2. Ramp generator, clock and buffers.
3. Phase reference and phase-shift control circuit (with interfaces) and J-K flip flops.
4. Triangular waveshape generator and buffers.
5. Voltage error amplifier, full wave rectifier and 180 degrees limit circuit.
6. Phase detector circuit with "clear" and hold-off circuit.
7. Phasing guarantee circuit.
8. Supply voltage regulators.

Each of the corresponding subcircuits is shown on the main schematic and marked with the same number.

5.1 THE POWER STAGE, THE DRIVER STAGE AND THE ACTIVE OFF-BIAS CIRCUIT

The output power stage consists of the inductor-transformer TI, resonant capacitors C15 and C16, feed-choke L and main transistor switches Q5 and Q6.

As the operation of this stage has already been discussed in detail no further explanation is offered here. The winding specifications of the magnetic components are however included in the appendix.



Notes

Unless Otherwise Specified:

1.) All resistors are ±5%, 1/4 W, ABC
2.) All capacitors are in μF
3.) All diodes are IN4447
4.) Z10 is Harris CMOS
5.) All IC's with "HA" prefix are Harris Linear
6.) All IC's with "MC" prefix are Motorola
7.) Z1 is National
8.) All other IC's are T.I. SN7400 Series
9.) Highest Reference Designations Used:
R126 CR34 Q17
C30 Z20

IC Power and Ground Pin Connections

	+15V	-15V	+10V	+5V	Gnd
Z1	4	11	—	—	—
Z2	14	7	—	—	—
Z3	14	7	—	—	—
Z4	11	6	—	—	2
Z5	11	6	—	—	2
Z6	14	7	—	—	—
Z7	14	7	—	—	—
Z8	14	7	—	—	—
Z9	14	7	—	—	—
Z10	—	—	14	—	7
Z11	—	—	—	14	7
Z12	14	7	—	—	—
Z13	—	—	—	14	7
Z14	—	—	—	14	7
Z15	—	—	—	14	7
Z16	—	—	—	5	13
Z17	—	—	—	14	7
Z18	14	7	—	—	—
Z19	As Shown	—	—	—	As Shown
Z20	—	As Shown	—	—	As Shown

FIGURE 5-1. Current-Fed Inverter

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The driver stage consists of the driver transformer T3, the clamping transistors Q1 and Q2 and the on-bias resistors R31 and R34. Driver transformer T3 utilizes self-regenerative feedback by sensing the collector currents of the main switches and adjusting the base drive proportional to the collector current. Any unnecessary overdrive power with its associated losses is thus avoided.

Current control resistor R43 allows for proper clamping and turn-off of the driver transformer and delivers excitation current only.

The active off-bias circuit with capacitor C12, off-bias transistors Q5 and Q6, trigger capacitors C13 and C14, rectifying diodes CR19 and CR20 and steering diodes CR15, 16 and CR17, 18 not only assures fast turn-off of the main transistors but also prevents the momentary turn-on of the off-transistors whenever the conducting transistor is turned off.

Capacitor C12 is charged through centertap-full wave rectification to a DC voltage level equal to V_{BE} of the main transistor plus one diode drop. Upon turn-off of one of the main transistors this voltage is back-biasing the base-emitter junction of the main transistors Q5 and Q6′ through the off bias transistors Q3 and Q4 respectively. The latter transistors are controlled by the lagging edge of the on-pulse to the main transistors. The rectangular on-pulses are differentiated through two RC networks C10/R35 and C11/R36, inverted by the pulse transformers T1 and T2 and then coupled capacitively to the bases of the transistors Q3 and Q4.

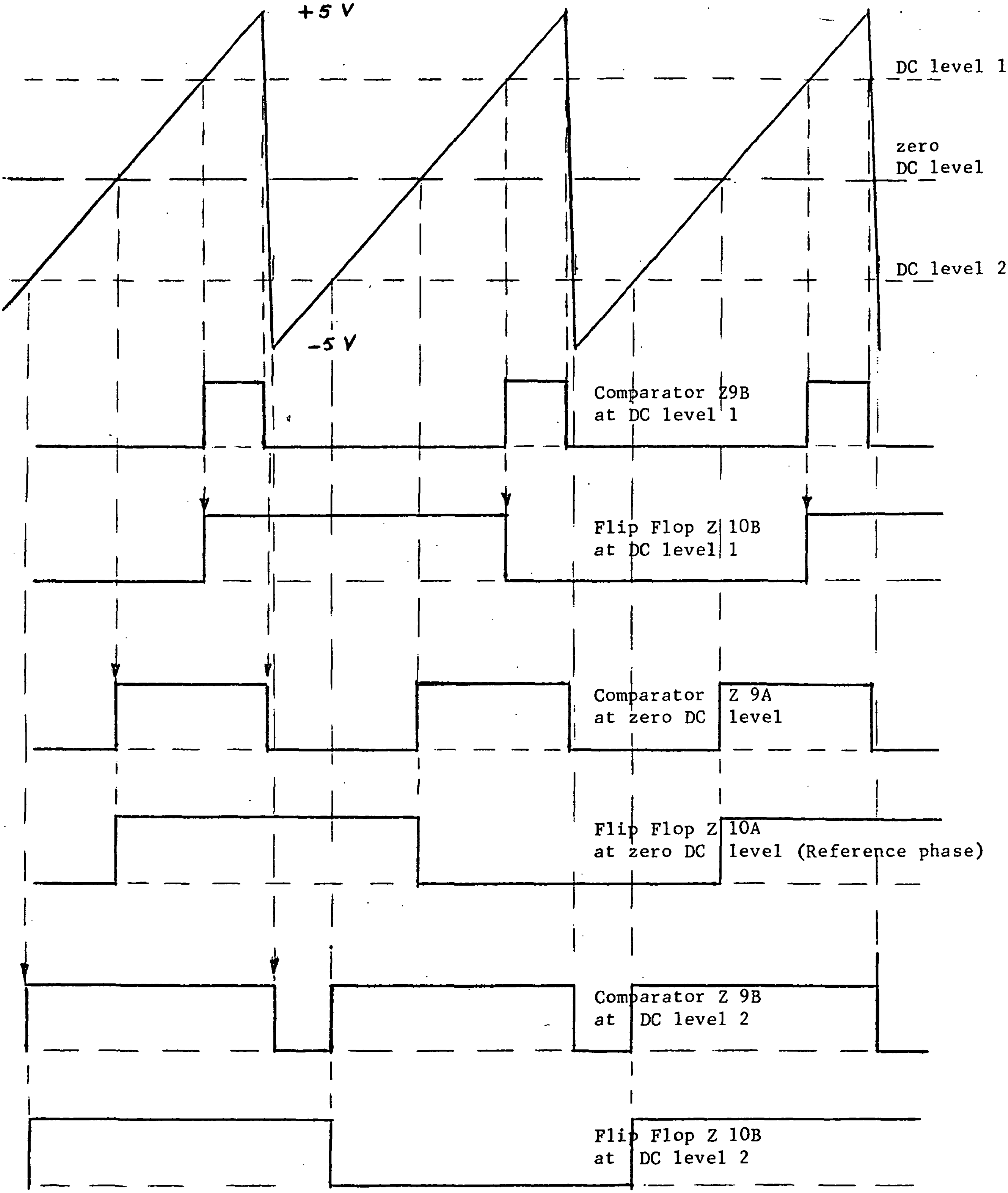
5.2 RAMP GENERATOR, CLOCK AND BUFFERS

The ramp generator consists of two operational amplifiers Z6A and Z6B. The first operational amplifier Z6A is an integrator with a capacitance of 0.01 μF and different charge and discharge paths. Capacitor C18 is discharged linearly due to a large time-constant established through the resistor R50 with a value of 24 kΩ. During the reverse input polarity compacitor C18 is connected through diode to resistor R49 with a value of 510Ω. Recharging of the capacitor is therefore about 50 times faster. The output voltage swing of the integrator is controlled by the zero crossover detection operational amplifier Z6B with a designed-in hysteresis of ±7.5 volts. In the breadboard configuration the free-running ramp generator is also the frequency determining element for the current-fed inverter. External synchronization of the ramp generator is possible but not recommended for the final breadboard. Even though correct frequency synchronization can be maintained easily exact phase lock is not always assured. A different circuit approach is therefore shown in figure 6-1.

The output of the ramp-generator is fed into two buffers Z7A and Z7B to assure proper operation of the following comparators Z9A and Z9B.

5.3 REFERENCE PHASE, PHASE SHIFT CONTROL CIRCUIT AND J-K FLIP-FLOPS

The generation of the reference phase and the phase-shiftable square wave are accomplished through the use of comparators Z9A/Z9B, J-K flip-flops Z10A/Z10B and the comparison of DC voltage levels with the ramp generator waveshape. The timing diagram of figure 5-2 shows for DC levels 1 and 2 which are superimposed on the ramp voltage waveform the corresponding comparator output signals and the resulting outputs of the J-K flip-flop Z9B. The timing diagram also shows the output of the zero crossover detection comparator Z9A and the corresponding reference phase as generated by the J-K flip-flop Z10A.



Timing diagram of ramp generator, reference square wave and phase shiftable square wave

Figure 5-2

A comparison of the signals generated by the DC levels 1, 2 and zero shows that leading and lagging square waves will be generated which can be shifted ±90 degrees with respect to the reference phase.

Transistors Q7 and Q8 are required as interface between the comparators and the CMOS J-K flip-flops. Transistor Q9 inverts the pulse train and yields a 90 degrees phase shift which becomes a requirement when the triangular voltage waveshape is derived by integration from the square wave. (See under 4).

To assure properly phased operation of the J-K flip-flops Z10A and Z10B a "clear" signal is applied. This "clear" signal is generated in the "phase guarantee circuit." The operation of this circuit is described in Section 7.

5.4 THE TRIANGULAR VOLTAGE WAVESHAPE GENERATOR WITH BUFFERS AND THE PULSEWIDTH MODULATOR

The triangular voltage waveshape is derived from the output of the phase-shiftable J-K flip-flop Z10B. The output of the J-K flip-flop is coupled capactively into the integrator Z1C. Stabilization is enhanced through negative DC feedback through R23. The symmetrical output of the integrator drives through capacitor C6 two buffer amplifiers Z3A and Z3B. These buffers generate at unity gain a non-inverted and an inverted replica of the input waveshape and allow to generate pulsewidth modulation at 180 degrees intervals.

Pulsewidth modulation is accomplished by comparing in the comparators Z4 and Z5 the levels of the triangular waveshapes from Z3A and Z3B with a variable DC level from the output of the error amplifier Z2A and the 180 degrees clamp Z2B. Varying the DC levels between zero and the peak value of the triangular voltage waveshape allows pulsewidth modulation between 0 and 180 degrees.

The pulsewidth modulated outputs of the comparators drive the clamp transistors Q1 and Q2 of the driver circuit. (See Section 1).

It is appropriate to mention that comparators with their high gain and their fast slewing rate exhibit a tendency of creating a jitter when a DC level is compared with a relative slow ramp waveshape. A detailed description of this phenomenon is presented in Texas Instruments' book, "Linear and Interface Circuits Application 1974" under the section, "Comparators," pages 108 to 111.

5.5 FULL WAVE RECTIFIER VOLTAGE ERROR AMPLIFIER AND 180 DEGREE LIMIT CIRCUIT

The sensing of the output voltage of the inverter is performed by the error amplifier Z2A after the sinusoidal output voltage has been attenuated by resistors R1 and R2 and after it has been rectified by the "full-wave perfect rectifier" consisting of operation amplifiers Z1A and Z1B. The term "perfect rectifier" has been assigned to this rectifying and integrating circuit because it avoids diode voltage drops during the conversion process. Without the integrating capacitor C1 the output at point C in figure 5-1 would follow the input within millivolts except that the negative half of the sinewave has been inverted. During the negative half cycle of the sinewave operational amplifier Z1A inverts the sinewave and takes Z1A out of action with respect to Z1B. During the positive half-cycle of the sinewave both operational amplifiers are active. The output at point C is therefore a fully rectified signal of equal amplitude as the average of the AC input signal.

During testing it was discovered that some spurious spikes were still present at point C and additional filtering through R12 and C2 was added.

The output signal of the perfect rectifier is compared in the error amplifier with the reference voltage across zener diode CR3. Any error signal is amplified by Z2A and controls, after passing through the 180 degree clamp, the pulsewidth modulation Z3A and Z3B.

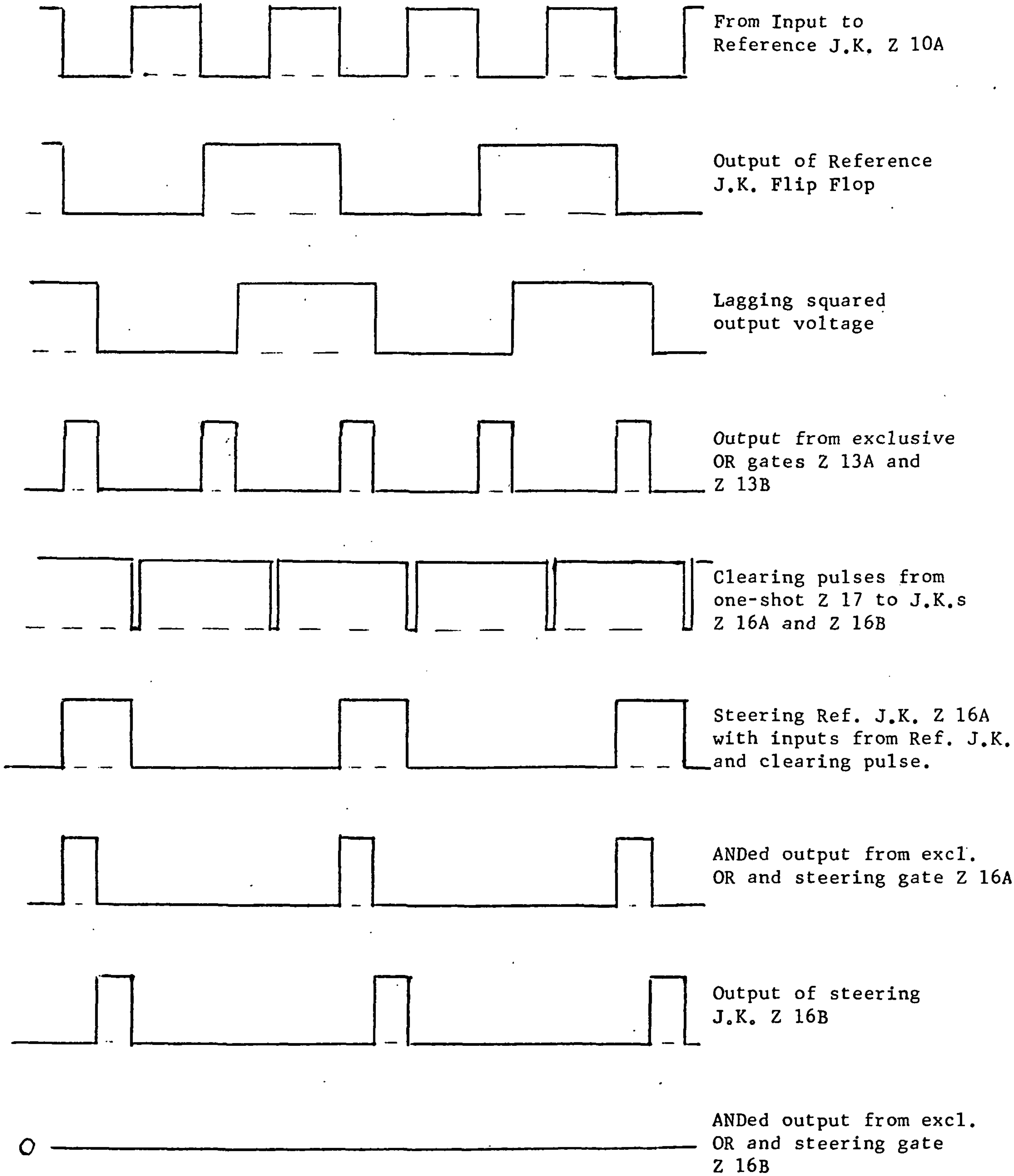
The 180 degree clamp circuit is actually a voltage follower with unity gain which cannot generate negative voltages. Because of these characteristics it prevents the comparators from generating pulsewidths in excess of 180 degrees. This circuit performs therefore a strictly protective function and prohibits overlapping conduction times of the main and the clamp transistors.

5.6 THE PHASE DETECTOR CIRCUIT WITH CLEAR-AND HOLD-OFF CIRCUITS

The input signals to the phase detector are the square wave from the J-K flip-flop Z10A which generates the reference phase and a square wave which is in phase with the AC output voltage. This square is generated by sensing the output voltage with a series combination of a resistor R94 and two diodes back to back in parallel, CR32 and CR33. The two diodes perform the initial squaring and the voltage across them is then driving the operational amplifier Z12A. The latter one assures properly shaped square waves with fall times of less than 100 nanoseconds. A transistor interface (Q14) circuit feeds the signal into the phase detector circuit.

Figure 5-3 shows the timing diagram when the output voltage lags the reference phase. The steering J-K flip-flops Z16A and Z16B are controlled by the reference phase and the output phase respectively and the one shot Z17 which is controlled by the input to the reference J-K flip-flop Z10A. The clearing pulses from the one shot Z17 have a duration of 20 μsec, occur at the 90 degrees and the 270 degrees points of the reference phase and allow to properly steer leading and lagging indicating pulses into the respective integrators Z18A and Z18B.

Between the AND gates Z14A and Z14B and the two integrators two more AND gates Z15A and Z15B are inserted which cause a delay in feeding the phase relation to the integrators. This delay or hold-off is caused by the delayed turn on of transistor Q15 and assures that phasing information is going to the integrators only when both the reference phase and the



Timing diagram of phase detector when output phase lagging reference phase

Figure 5-3.

squared output voltage phasing have been established. This causes the output power stage's base drive to initially turn-on in phase with the reference phase.

Integrators Z18A and Z18B generate a positive or negative output voltage depending on which integrator is activated. Their output voltages are summed at point D and thus generate positive and negative going voltage depending on whether leading or lagging phase shifts are detected.

This output voltage is the phase controlling signals into the operational amplifier Z7B which in comparator Z9B shifts the pulses to control the phase-shiftable J-K flip-flop Z10B.

Attenuating the output voltage from the operational amplifier Z7B limits the maximum possible phase shift to ± 90 degrees or less.

5.7 CORRECT PHASING ASSURANCE CIRCUIT

It was pointed out before that the high gain and the fast slew rate of the comparators Z4 and Z5 can easily cause incorrect phasing of the following J-K flip-flops. Instead of being in phase Z4 and Z5 were 180 degrees out of phase. As this condition represents an unacceptable danger a correct phase assurance circuit was incorporated. This circuit assures correct phasing, even under phase shift conditions of ± 90 degrees by momentarily clearing through transistor Q10 the J-K flip-flops Z10A and Z10B with a pulse of about 20 microseconds.

The correct phasing assurance ciruit consists of two AND gates Z14C and Z14D, one IC inverter Z11A and one inverter and interface circuit with transistor Q13.

The correct phasing assurance circuit gets its three input signals A, B and C from the reference comparator clock signal (pin 12 on Z10A), the actual output phase signal from the collector of Q12 and the output of phase detector gate Z14B, pin 6 respectively.

A correcting clear signal is produced when the three signals produce a "high" at the output of AND gate Z14D: $Y = \bar{A}\ \bar{B}\ C$

5.8 THE SUPPLY VOLTAGES

During the breadboard testing all power for the current-fed inverter and its control circuit was supplied from external sources. Only for the required plus and minus 15 volt DC were extra IC voltage regulators (Z19 and Z20) incorporated.

In a final circuit and during start-up all voltages would be derived from the main input supply. After start-up all power for the control circuits would be derived from the regulated output of the current-fed inverter.

To properly account for the losses the test data lists losses and efficiencies with and without the inclusion of the control circuit losses.

SECTION 6

EVALUATION AND SUMMARY OF THE TEST RESULTS

6.1 BREADBOARD TEST RESULTS

The breadboard test results are presented in the following six tabulations which were measured at three input voltage levels, four power factor settings and three selected load points. Power factor readings were taken both at capacitive and inductive power factors.

It is important to note that all readings were taken at a regulated output voltage of 45V ac and NOT at the specified 50V ac. As the power levels however were maintained all output currents are approximately 10 percent higher and their associated copper losses about 20 percent higher. As a consequence the overall and the output stage efficiencies are lower than those if the output voltage had been 50V ac.

Inspection of the test results also indicates that the losses increase as the input voltage increases. This characteristic is caused by an increase in the firing angle α which causes an increased current to flow through the secondary winding of the feed-choke L. Equation -15 indicates that the RMS current through the secondary winding of L increases with the root of α and the losses therefore increase proportional to α. At a firing angle $\alpha = 0$, which occurs at the lowest input voltage, there are no losses in the secondary winding of the feed-choke L.

All tests were performed at room temperature only because of the lack of time.

Part of the testing was limited by a lack of inductance values and also by instabilities at certain test points.

From the six main tabulations nine loss-and efficiency curves are plotted and six tabulations show output regulation under capacitive and inductive loading, output-distortion under capacitive and inductive loading and output phase error under capacitive and inductive loading.

The test data indicates when compared against the statement of work that:

a. The breadboard operates over the specified input voltage range of 25 to 50V dc.

b. The breadboard maintains output voltage regulation against line and load changes at an output voltage of 45V ac at better than $45.35 \pm 0.45 = 45.35 \pm 1\%$. (45.8 to 44.9V ac). The statement of work specifies output voltage regulation against line, load and temperature changes at 50V RMS $\pm 3\%$.

   NOTE: The test data were measured at an output voltage of ≈ 45 volts because the inductor-transformer TI had not yet been modified to properly operate at an output voltage of 50V ac.

c. The output voltage waveform's maximum distortion over the full load, full power factor and full input voltage range is equal or better than 7.8 percent and thus lower than the specified 10 percent total Harmonic Distortion.

d. The inverter can easily handle power factors beyond those specified at ± 0.7.

e. The overall maximum efficiency of the breadboard inverter is 85.3 percent. This value is less than the specified 88 percent. One has, however, to keep in mind that due to the reduced output voltage the output copper losses are 20 percent higher than at normal output voltage and that no optimization was undertaken.

f. The breadboard was tested at room temperature only and not over the specified temperature range of 0^{o} to $75^{o}C$.

g. The transient response was not further investigated as the circuit still has points of instability.

h. The voltage phase lock against line-load-and power-factor changes was equal to or better than 1 degree.

i. The operating frequency of the inverter was 2460 ± 3 Hz. Even though the inverter was not tested over the specified temperature range no problems are expected in meeting the specified tolerance of $2400 \pm 5\%$ Hz.

   NOTE: Due to the non-availability of sufficient inductance values no test data were taken at 200 VA and a lagging power factor of 0.7.

Power Factor	VA	E in (VDC)	I in (ADC)	Pin (Watts)	Pcontrol (Watts)	e_{out} (Vrms)	R_L (Ω)	C (μF)	L (mH)	Pout $\frac{e^2}{R_L}$ (Watts)	Distortion (%)	Phase Error (degrees)	Freq. (Hz)	Overall Efficiency (%)	Power Stage Efficiency (%)
1.0	200	50.00	5.12	256	3.8	45.6	10.13	—	—	205.3	5.3	0	2463	79.0	80.2
	135	50.00	3.29	164.5	3.8	45.6	15.01	—	—	138.5	4.2	0	2464	82.3	84.2
	65	50.00	1.58	79.00	3.8	45.6	31.27	—	—	66.50	2.9	0	2463	80.3	84.2
0.9	200	50.00	4.80	240.0	3.8	45.6	11.36	2.79	—	183.0	4.4	0.6	2464	75.1	76.3
	135	50.00	3.15	157.5	3.8	45.6	11.68	1.91	—	124.7	3.5	0.6	2464	77.3	79.2
	65	50.00	1.51	75.50	3.8	45.7	34.58	0.88	—	60.40	2.2	0.6	2464	76.2	80.0
0.8	200	50.00	4.50	225.0	3.8	45.8	12.67	3.82	—	165.6	4.6 *	0.8 *	2464	72.4	73.6
	135	50.00	2.94	147.0	3.8	45.8	18.65	2.59	—	112.5	3.7 *	0.8 *	2464	74.6	76.5
	65	50.00	1.41	70.50	3.8	45.8	38.84	1.30	—	54.01	2.3 *	0.8 *	2464	72.7	76.6
0.7	200	Unstable above 45V Ein													
	135	50.00	2.68	134.0	3.8	45.8	21.68	3.13	—	96.76	4.3 *	Marginally stable (≈1°)	2465	70.2	72.2
	65	50.00	1.29	64.50	3.8	45.8	44.09	1.52	—	47.58	2.6 *	Marginally stable (≈1°)	2463	69.7	73.8

Capacitive Loading

* Jittery but not unstable. Distortion readings may not be not accurate,

Power Factor	VA	E_{in} (VDC)	I_{in} (ADC)	P_{in} (Watts)	$P_{control}$ (Watts)	e_{out} (V_{rms})	R_L (Ω)	C (μF)	L (mH)	P_{out} $\frac{e_o^2}{R_L}$ (Watts)	Distortion (%)	Phase Error (degrees)	Freq. (Hz)	Overall Efficiency (%)	Power Stage Efficiency (%)
1.0	200	37.50	6.42	240.8	3.8	45.3	10.13	—	—	202.6	3.8	0	2463	82.9	84.2
	135	37.50	4.20	157.5	3.8	45.3	15.01	—	—	136.7	2.6	0	2463	84.8	86.8
	65	37.50	2.02	75.75	3.8	45.3	31.27	—	—	65.63	1.7	0	2463	82.5	86.6
0.9	200	37.50	5.90	221.3	3.8	45.5	11.36	2.79	—	182.2	2.8	0.5	2463	81.0	82.4
	135	37.50	3.94	147.8	3.8	45.5	16.68	1.91	—	124.1	2.1	0.5	2463	81.9	84.0
	65	37.50	1.92	72.00	3.8	45.4	34.58	0.88	—	59.61	1.2	0.5	2463	78.6	82.8
0.8	200	37.50	5.47	205.1	3.8	45.6	12.67	3.82	—	164.1	2.9 *	0.8 *	2465	78.5	80.0
	135	37.50	3.67	137.6	3.8	45.6	18.65	2.59	—	111.5	2.4 *	0.8 *	2463	78.8	81.0
	65	37.50	1.78	66.75	3.8	45.6	38.24	1.30	—	53.54	1.5 *	0.8 *	2463	75.9	80.2
0.7	200	37.50	5.09	190.9	3.8	45.6	14.71	4.57	—	141.4	3.6 *	1.1° *	2464	72.6	74.1
	135	37.50	3.34	125.3	3.8	45.6	21.65	3.13	—	95.91	3.0 *	[illegible]	2465	74.3	76.6
	65	37.50	1.63	61.13	3.8	45.6	44.09	1.52	—	47.16	1.9 *	0.9 *	2463	72.6	77.2

Capacitive Loading

* Jittery but not unstable.

Distortion readings may not be accurate.

Power Factor	VA	E_{in} (VDC)	I_{in} (ADC)	P_{in} (Watts)	$P_{control}$ (Watts)	e_{out} (V_{rms})	R_L (Ω)	C (μF)	L (mH)	P_{out} $\frac{e_o^2}{R_L}$ (Watts)	Distortion (%)	Phase Error (degrees)	Freq. (Hz)	Overall Efficiency (%)	Power Stage Efficiency (%)
1.0	200	25.00	9.51	237.8	3.8	45.0	10.13Ω	—	—	199.9	7.8%	0°	2457	82.7	84.1
	135	25.00	6.24	156.0	3.8	44.9	15.01Ω	—	—	134.3	5.1%	0°	2457	84.0	86.1
	65	25.00	3.02	75.5	3.8	45.0	31.27Ω	—	—	64.76	2.4%	0°	2455	81.7	85.8
0.9	200	25.00	8.22	205.5	3.8	45.0	11.36Ω	2.79	—	178.3	5.1%	0.4°	2457	85.2	86.7
	135	25.00	5.54	138.5	3.8	45.0	16.68Ω	1.91	—	121.4	3.8%	0.4°	2457	85.3	87.7
	65	25.00	2.74	68.50	3.8	45.0	34.58Ω	0.88	—	58.56	2.2%	0.3°	2459	81.0	85.5
0.8	200	25.00	7.56	189.0	3.8	45.0	12.67Ω	3.82	—	159.8	3.8%	0.65°	2458	82.9	84.6
	135	25.00	5.14	128.5	3.8	45.1	18.65Ω	2.59	—	109.1	2.9%	0.65°	2459	82.5	84.9
	65	25.00	2.52	63.00	3.8	45.1	38.84Ω	1.30	—	52.37	1.5%	0.6°	2457	78.4	83.1
0.7	200	25.00	7.08	177.0	3.8	45.1	14.71Ω	4.57	—	138.3	2.6%	0.9°	2458	76.5	78.1
	135	25.00	4.66	116.5	3.8	45.2	21.68Ω	3.13	—	94.24	2.0%	0.9°	2457	78.3	80.9
	65	25.00	2.30	57.50	3.8	45.2	44.09Ω	1.52	—	46.34	1.0%	0.8°	2458	75.6	80.6

Capacitive Loading

Power Factor	VA	E in (VDC)	I in (ADC)	P in (Watts)	P control (Watts)	E out (Vrms)	R_L (Ω)	C (μF)	L (mH)	P out $\frac{e_o^2}{R_L}$ (Watts)	Distortion (%)	Phase Error (degrees)	Freq. (Hz)	Overall Efficiency (%)	Power Stage Efficiency (%)
0.9	151	50.00	3.40	170.0	3.8	45.6	14.9	—	2	139.6	5.7	0.3	2464	80.3	82.1
	101	50.00	2.25	112.5	3.8	45.6	22.4	—	3	92.8	4.4	0.3	2464	79.8	82.5
	75	50.00	1.70	85.0	3.8	45.6	29.8	—	4	69.8	3.7	0.3	2464	78.6	82.1
0.8	110	50.00	2.29	114.5	3.8	45.7	22.1	—	2	90.46	5.1	0.4	2464	76.5	79.0
	73	50.00	1.53	76.5	3.8	45.7	34.6	—	3	60.4	3.8	0.4	2464	75.2	78.9
	55	50.00	1.16	58.0	3.8	45.7	46.2	—	4	45.2	3.3	0.4	2464	73.2	77.9
0.7	92	50.00	1.77	88.5	3.8	45.7	31.4	—	2	66.50	4.7	0.6	2464	72.0	75.2
	61	50.00	1.19	59.5	3.8	45.7	47.1	—	3	44.34	3.5	0.5	2464	70.1	74.5
	46	50.00	0.91	45.5	3.8	45.7	62.8	—	4	33.26	3.1	0.4	2464	67.5	73.1

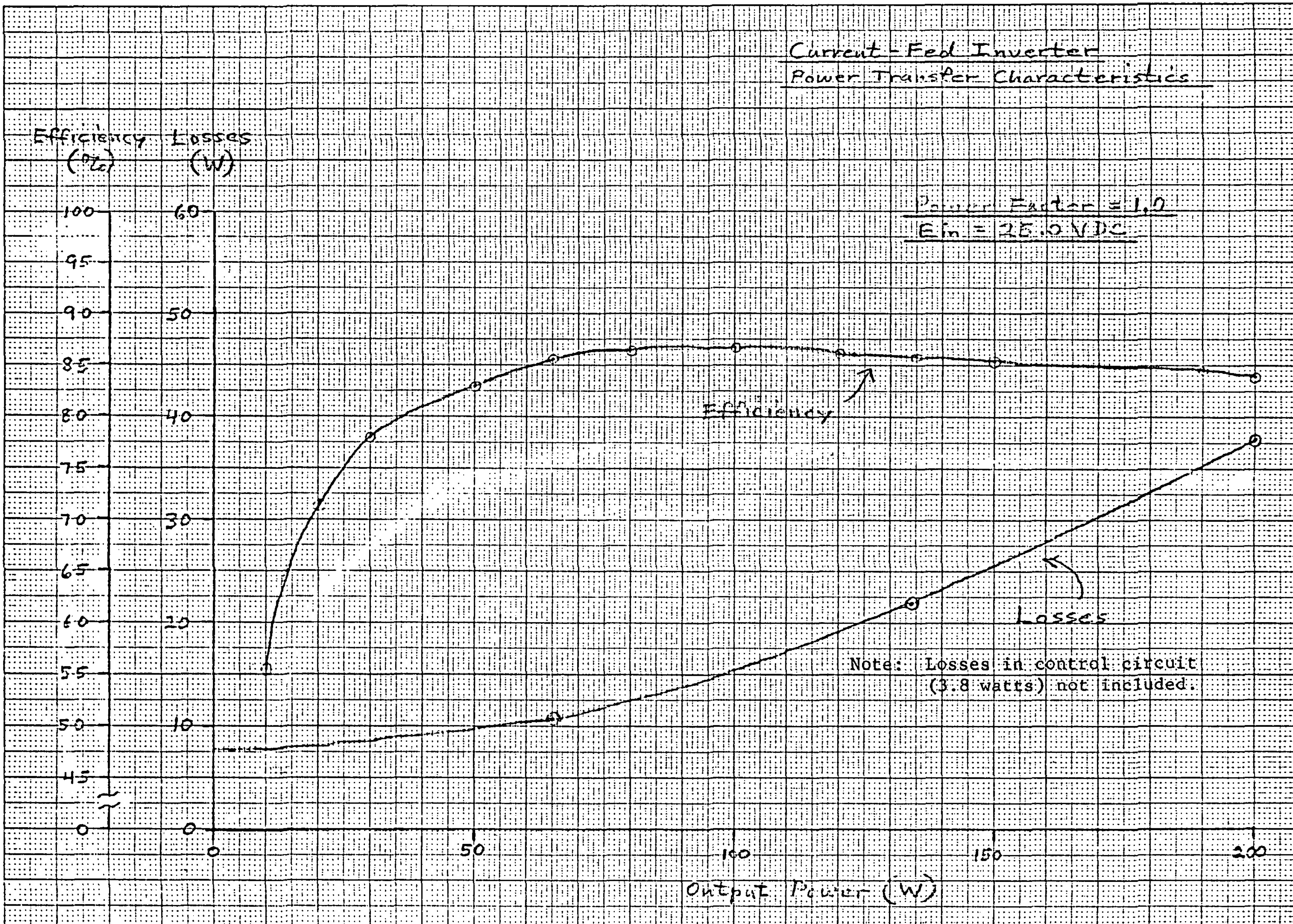
Inductive Loading

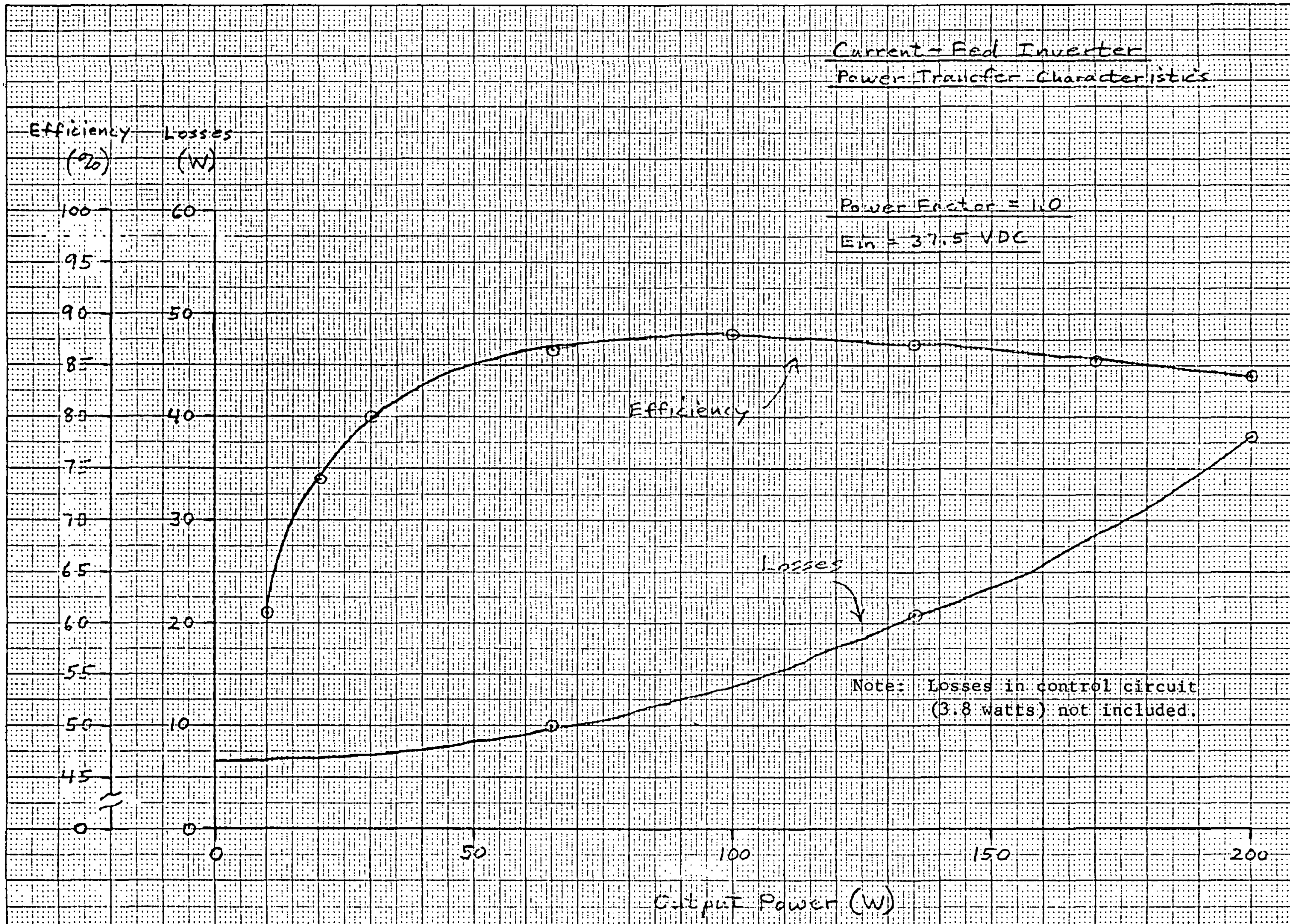
Power Factor	VA	E in (VDC)	I in (ADC)	P in (Watts)	P control (Watts)	e out (Vrms)	R_L (Ω)	C (μF)	L (mH)	P out $\frac{e_o^2}{R_L}$ (Watts)	Distortion (%)	Phase Error (degrees)	Freq. (Hz)	Overall Efficiency (%)	Power Stage Efficiency (%)
0.9	151	37.50	4.43	166.1	3.8	45.3	14.9	—	2	137.7	3.1	0.4	2464	81.0	82.9
	101	37.50	2.93	109.9	3.8	45.3	22.4	—	3	91.6	2.3	0.4	2464	80.6	83.4
	75	37.50	2.22	83.25	3.8	45.3	29.8	—	4	68.9	2.0	0.3	2464	79.2	82.7
0.8	110	37.50	2.97	111.4	3.8	45.5	23.1	—	2	89.6	3.0	0.5	2464	77.8	80.5
	73	37.50	2.00	75.0	3.8	45.4	34.6	—	3	59.6	2.15	0.5	2464	75.6	79.4
	55	37.50	1.51	56.6	3.8	45.4	46.2	—	4	44.6	1.8	0.4	2463	73.8	78.8
0.7	92	37.50	2.29	85.9	3.8	45.5	31.4	—	2	65.9	3.0	(≈0.7°) Marginal [illegible]	2464	73.5	76.8
	61	37.50	1.54	57.75	3.8	45.5	47.1	—	3	44.0	2.2	0.6	2464	71.5	76.1
	46	37.50	1.17	43.9	3.8	45.5	62.8	—	4	33.0	1.8	0.5	2464	69.2	75.2

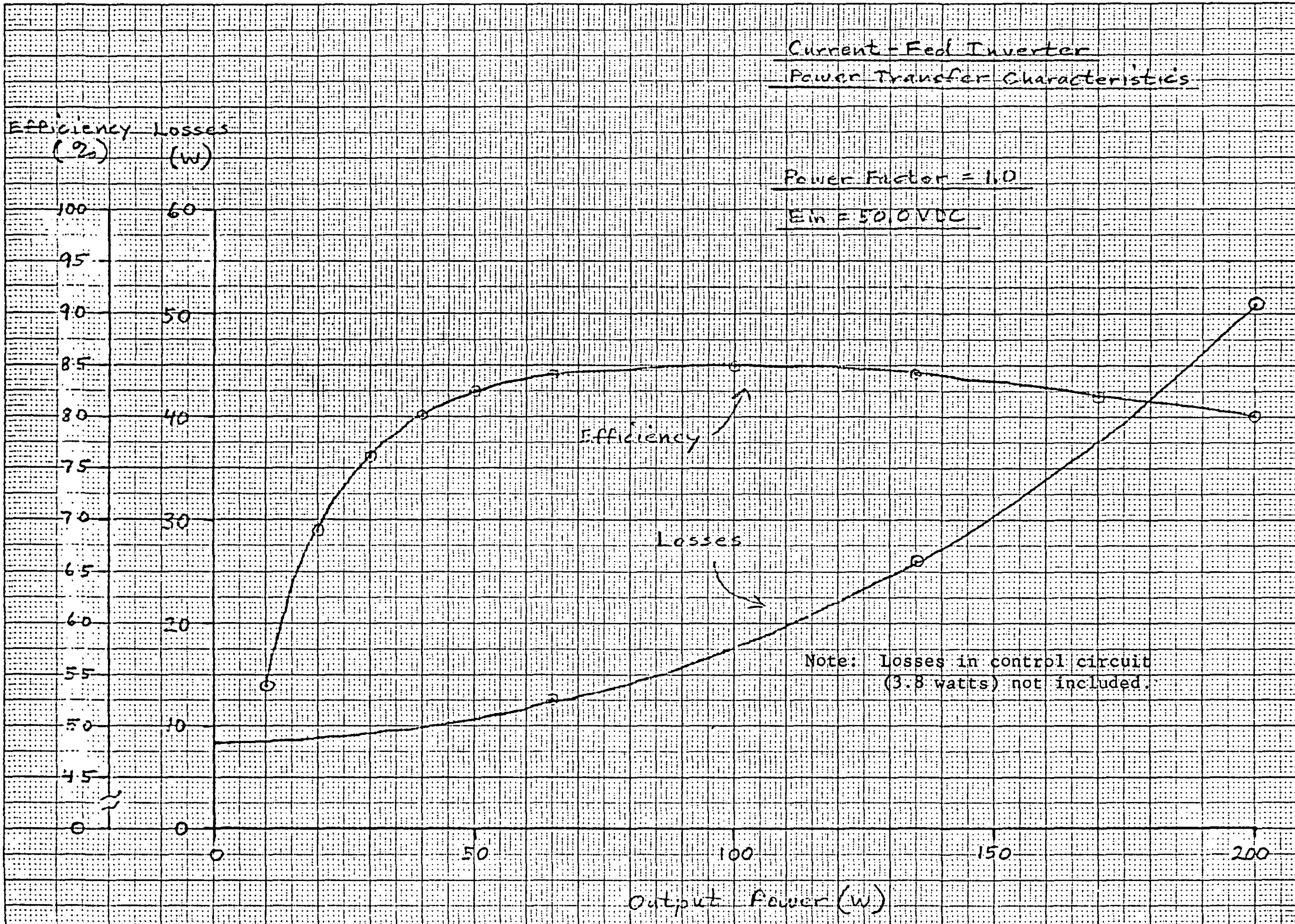
Inductive Loading

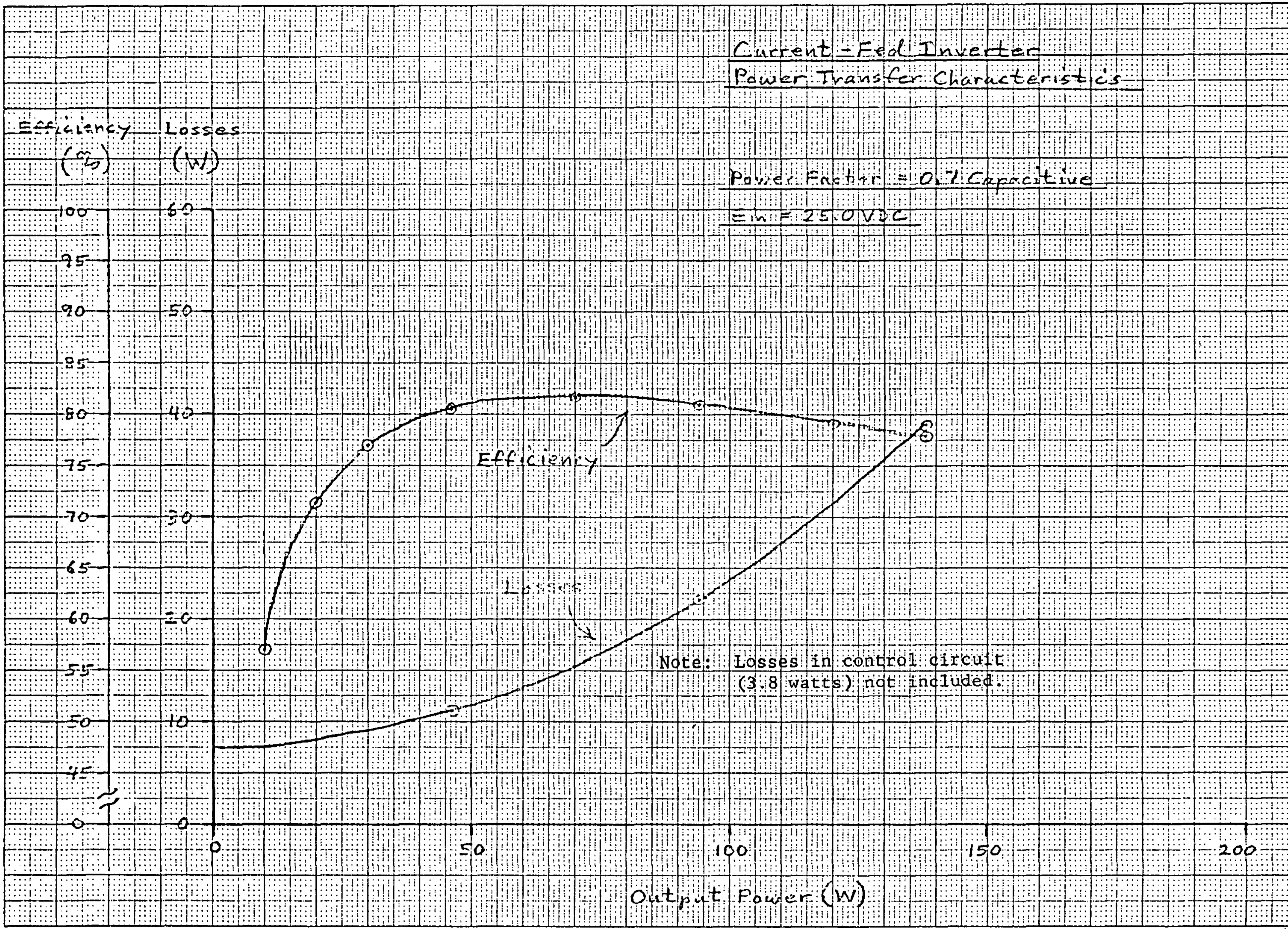
Power Factor	VA	E in (VDC)	I in (ADC)	P in (Watts)	P control (Watts)	e_{out} (Vrms)	R_L (Ω)	C (μF)	L (mH)	P_{out} $\frac{e_o^2}{R_L}$ (Watts)	Distortion (%)	Phase Error (degrees)	Freq. (Hz)	Overall Efficiency (%)	Power Stage Efficiency (%)
0.9	151	25.00	6.76	169.0	3.8	44.9	14.9	—	2	135.3	5.8	0.5	2464	78.3	80.1
	101	25.00	4.42	110.5	3.8	44.9	22.4	—	3	90.0	3.6	0.5	2464	78.7	81.5
	75	25.00	3.31	82.75	3.8	44.9	29.8	—	4	67.7	2.6	0.4	2463	78.2	81.8
0.8	110	25.00	4.42	110.5	3.8	45.0	23.1	—	2	87.66	3.6	0.7	2464	76.7	79.3
	73	25.00	2.96	74.0	3.8	45.1	34.6	—	3	58.80	2.3	0.6	2464	75.6	79.4
	55	25.00	2.22	55.5	3.8	45.1	46.2	—	4	44.03	1.7	0.6	2464	74.2	79.3
0.7	92	25.00	3.35	83.75	3.8	45.1	31.4	—	2	64.8	2.6	0.9	2464	74.0	77.3
	61	25.00	2.26	56.5	3.8	45.1	47.1	—	3	43.2	1.8	0.9	2464	71.6	76.4
	46	25.00	1.71	42.75	3.8	45.1	62.8	—	4	32.4	1.4	0.8	2464	69.6	75.8

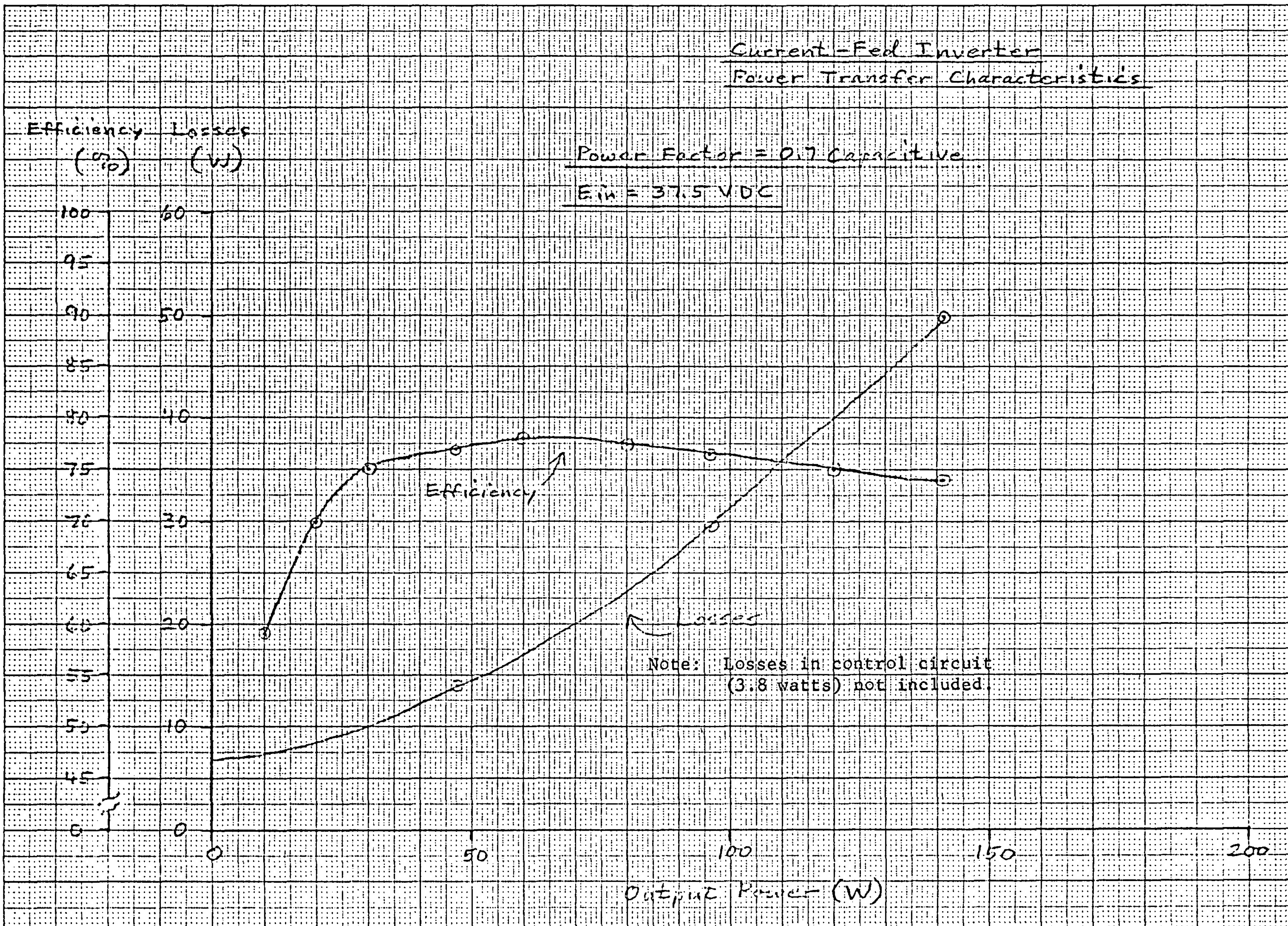
Inductive Loading

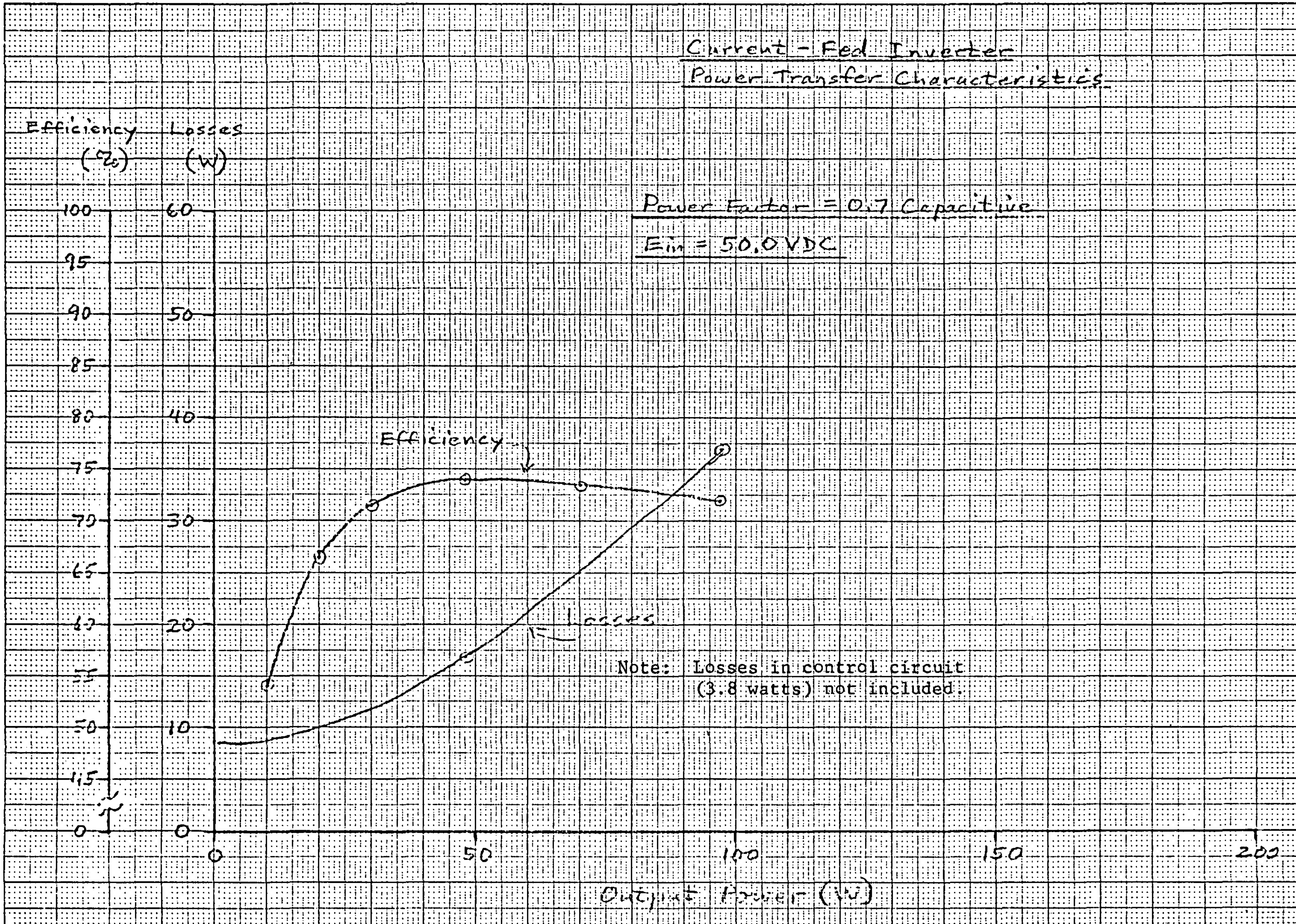

Current-Fed Inverter
Power Transfer Characteristics
Power Factor = 1.0
Ein = 25.0 VDC
Efficiency (%)
Losses (W)
100
95
90
85
80
75
70
65
60
55
50
45
0
60
50
40
30
20
10
0
0
50
100
150
200
Output Power (W)
Efficiency
Losses
Note: Losses in control circuit
(3.8 watts) not included.

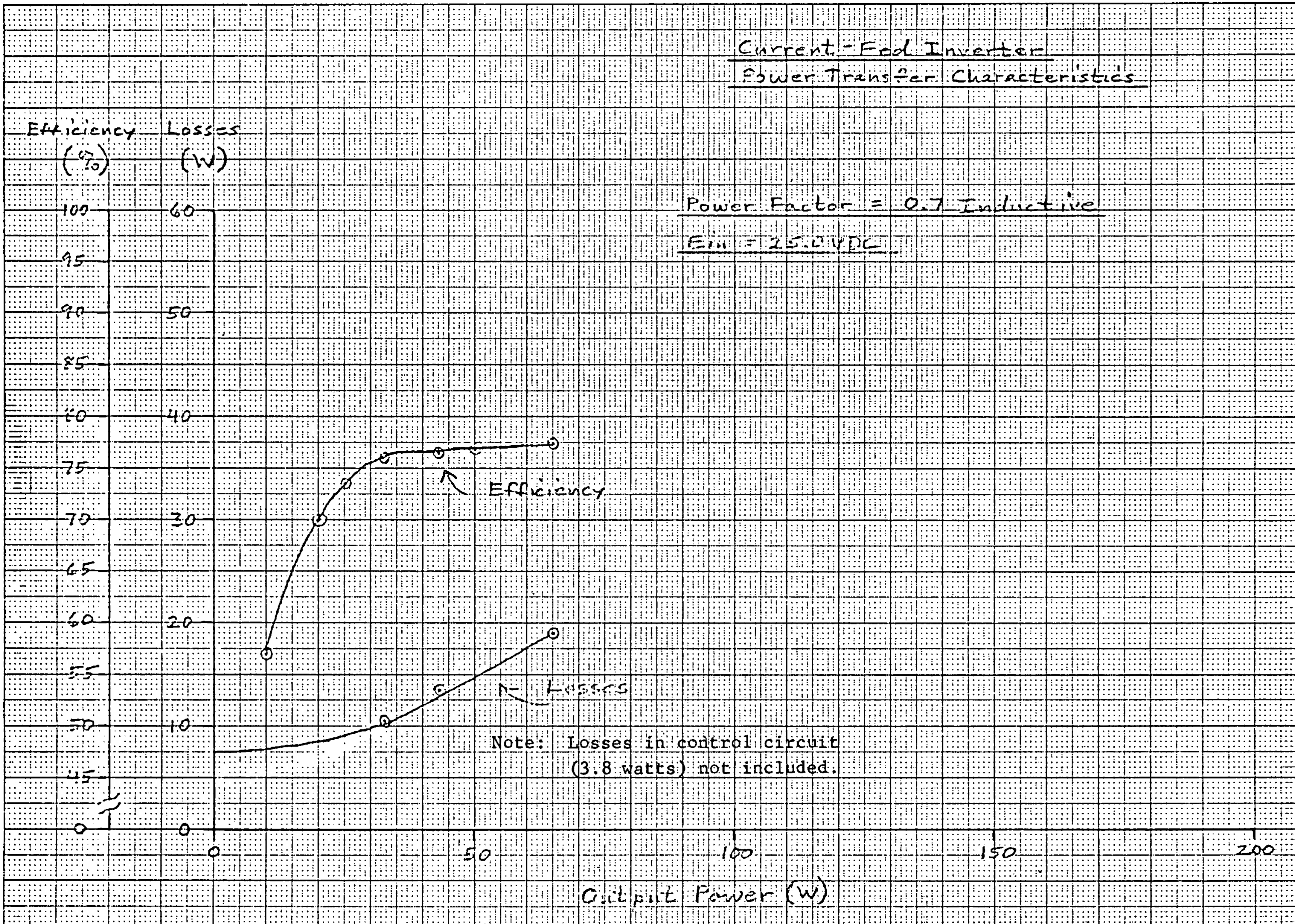

Current-Fed Inverter
Power Transfer Characteristics
Efficiency (%)
Losses (W)
Power Factor = 1.0
Ein = 37.5 VDC
100
95
90
85
80
75
70
65
60
55
50
45
0
60
50
40
30
20
10
0
Efficiency
Losses
Note: Losses in control circuit
(3.8 watts) not included.
0
50
100
150
200
Output Power (W)


Current - Fed Inverter
Power Transfer Characteristics
Power Factor = 1.0
Ein = 50.0 VDC
Efficiency (%)
Losses (W)
100
95
90
85
80
75
70
65
60
55
50
45
0
60
50
40
30
20
10
0
Efficiency
Losses
Note: Losses in control circuit (3.8 watts) not included.
0
50
100
150
200
Output Power (W)

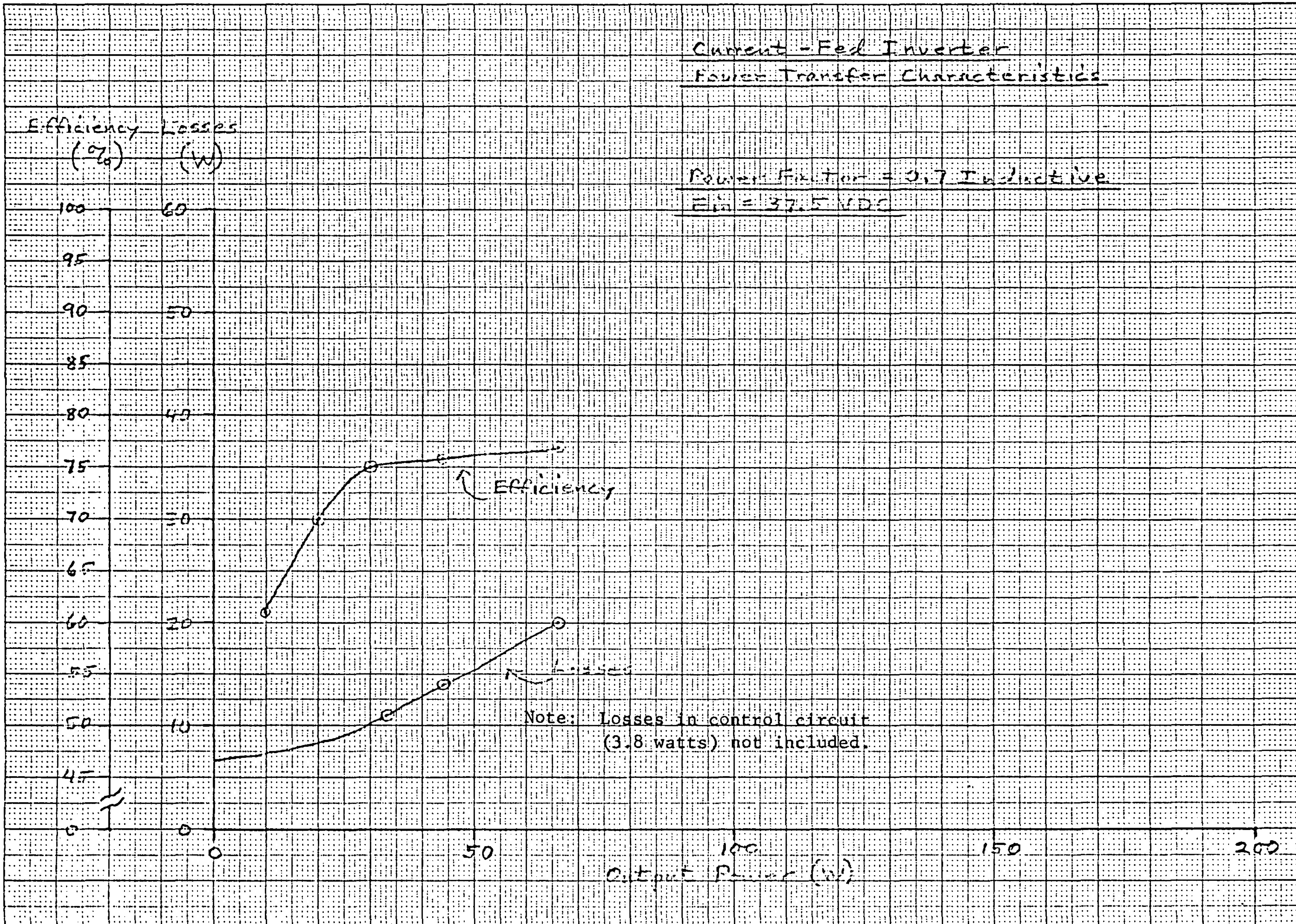

Current - Fed Inverter
Power Transfer Characteristics
Efficiency (%)
Losses (W)
Power Factor = 0.7 Capacitive
Ein = 25.0 VDC
100
95
90
85
80
75
70
65
60
55
50
45
0
60
50
40
30
20
10
0
Efficiency
Losses
Note: Losses in control circuit
(3.8 watts) not included.
0
50
100
150
200
Output Power (W)

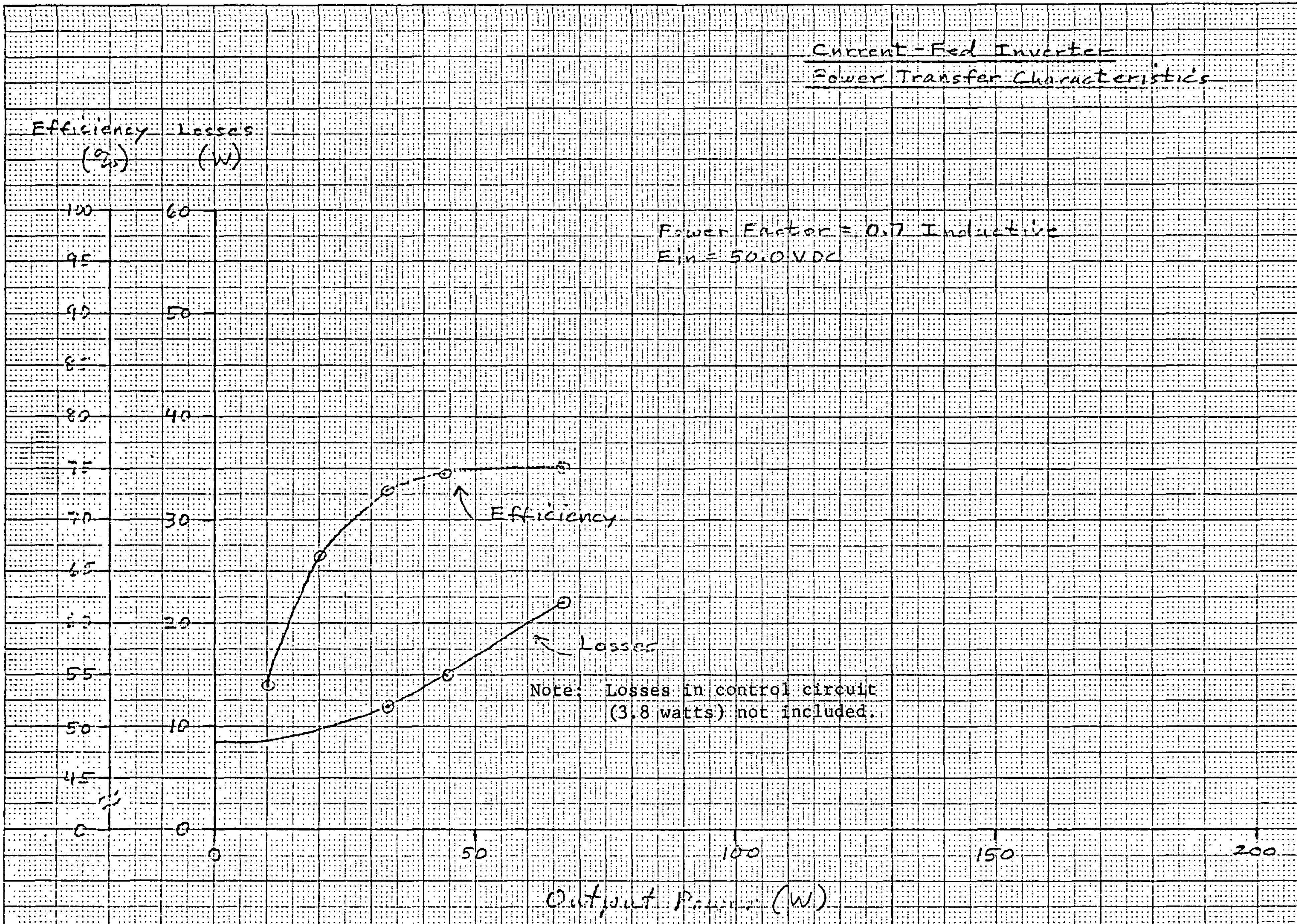

Current-Fed Inverter
Power Transfer Characteristics
Power Factor = 0.7 Capacitive
Ein = 37.5 VDC
Efficiency (%)
Losses (W)
100
95
90
85
80
75
70
65
60
55
50
45
0
60
50
40
30
20
10
0
Efficiency
Losses
Note: Losses in control circuit
(3.8 watts) not included.
0
50
100
150
200
Output Power (W)


Current - Fed Inverter
Power Transfer Characteristics
Efficiency (%)
Losses (W)
Power Factor = 0.7 Capacitive
E_{in} = 50.0 VDC
Efficiency
Losses
Note: Losses in control circuit (3.8 watts) not included.
Output Power (W)
100
95
90
85
80
75
70
65
60
55
50
45
0
60
50
40
30
20
10
0
0
50
100
150
200



Current-Fed Inverter
Power Transfer Characteristics
Power Factor = 0.7 Inductive
Efficiency (%)
Losses (W)
Efficiency
Losses
Note: Losses in control circuit (3.8 watts) not included.
Output Power (W)
0
50
100
150
200


Current - Fed Inverter
Power Transfer Characteristics
Power Factor = 0.7 Inductive
Ein = 37.5 VDC
Efficiency (%)
Losses (W)
Efficiency
Losses
Note: Losses in control circuit
(3.8 watts) not included.
Output Power (W)
0
50
100
150
200
100
95
90
85
80
75
70
65
60
55
50
45
60
50
40
30
20
10


Current-Fed Inverter
Power Transfer Characteristics
Efficiency (%)
Losses (W)
Power Factor = 0.7 Inductive
Ein = 50.0 VDC
Efficiency
Losses
Note: Losses in control circuit
(3.8 watts) not included.
100
95
90
85
80
75
70
65
60
55
50
45
0
60
50
40
30
20
10
0
0
50
100
150
200
Output
(W)

		e_{out}		
Output VA	E_{in}	PF = 1.0	PF = 0.7	% Δ
200	25 VDC	45.0 V	45.1 V	0.22
135	50 VDC	45.6 V	45.8 V	0.44
65	25 VDC	45.0 V	45.2 V	0.44
65	50 VDC	45.6 V	45.8 V	0.44

Worst-Case Δ E_{out} VS Line = 1.33 %
VS Load = 0.22 %
VS PF = 0.44 %
Combined = 1.78 %

Output Regulation With Capacitive Loading

		e_{out}		
Output VA	E in	PF = 1.0	PF = 0.7	% Δ
200	25VDC	45.0V	45.1V (92 VA)*	0.22
200	50VDC	45.6 V	45.7V (92VA)*	0.22
65	25 VDC	45.0V	45.1V (46VA)*	0.22
65	50 VDC	45.6 V	45.7V (46 VA)*	0.22

Worst-Case Δ Eout VS Line = 1.33 %
VS Load = 0 %
VS PF = 0.22 %
Combined = 1.56 %

*Note: Values in Output VA attainable with load combinations available.

Output Regulation With Inductive Loading

		Distortion	
Output VA	E in	PF = 1.0	PF = 0.7
200	25VDC	7.8 %	2.6 %
135	50VDC	4.2 %	4.3 %
65	25VDC	2.4 %	1.0 %
65	50VDC	2.9 %	2.6 %

Output Distortion With Capacitive Loading

		Distortion	
Output VA	E in	PF = 1.0	PF = 0.7
200	25VDC	7.8 %	2.6 % (92VA) *
200	50VDC	5.3 %	4.7 % (92VA) *
65	25VDC	2.4 %	1.4 % (46VA) *
65	50VDC	2.9 %	3.1 % (46VA) *

*Note: Values in Output VA attainable with load combinations available.

Output Distortion With Inductive Loading

		Phase Error	
Output VA	Ein	PF = 1.0	PF = 0.7
200	25 VDC	0°	0.9°
135	50 VDC	0°	1.0°
65	25 VDC	0°	0.8°
65	50 VDC	0°	1.0°

Output Phase Error With Capacitive Loading

		Phase Error	
Output VA	Ein	PF = 1.0	PF = 0.7
200	25VDC	0°	0.9° (92VA)*
200	50VDC	0°	0.6° (92VA)*
65	25VDC	0°	0.8° (46VA)*
65	50VDC	0°	0.4° (46VA)*

*Note: Values in Output VA attainable with load combinations available.

Output Phase Error With Inductive Loading

6.2 CONCLUSIONS FROM TEST RESULTS

The breadboard tests have proven that the current-fed inverter with phase-correcting loop for the base-drive of the main switches can meet all requirements for a successful three-phase system and maintain it even though any one phase might fail.

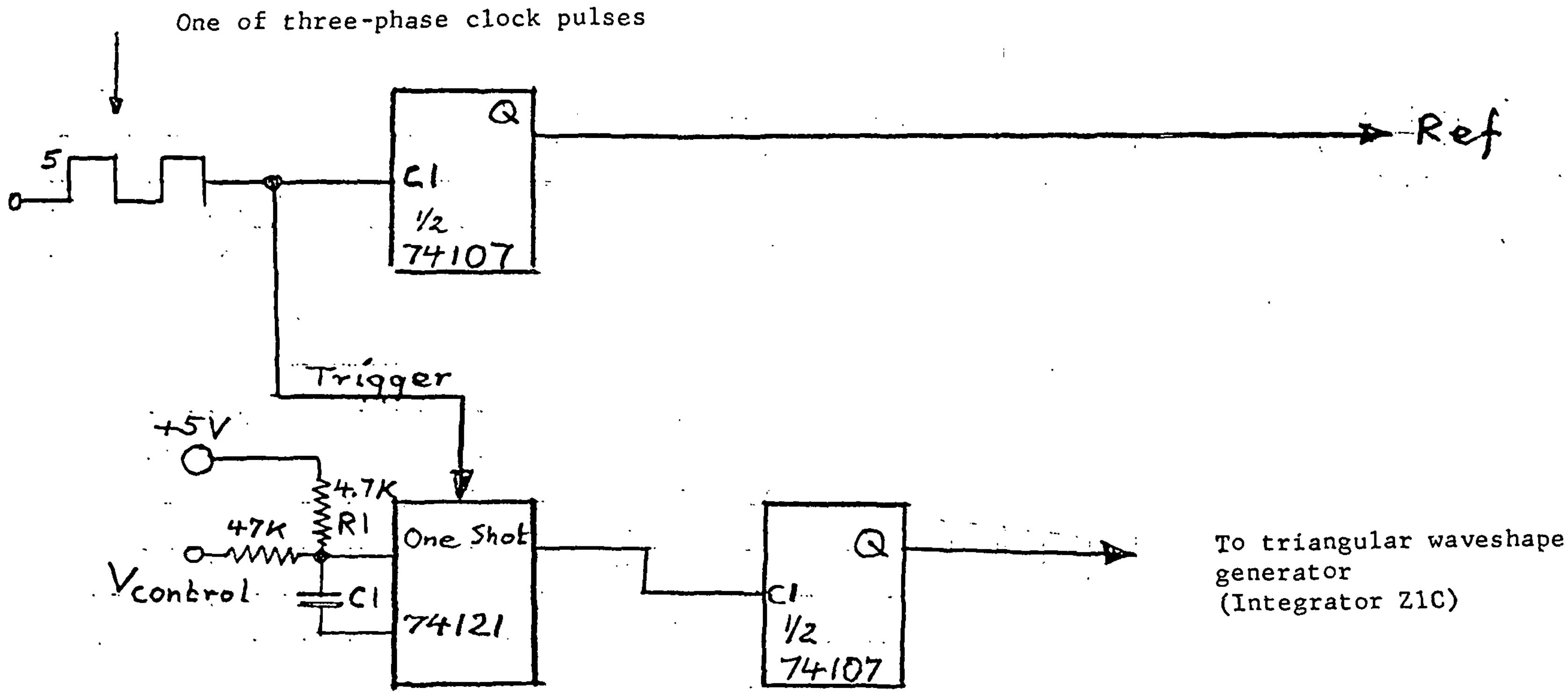
It is important to mention however that the breadboard had not been synchronized to a common clock with three-phase signals. This breadboard was free-running with its ramp-generator. As the ramp generator is easily synchronized in frequency but not uniquely in a fixed phase relation due to the count-down required in the present design, it is recommended that the front end be substituted with the following or a similar circuit. The proposed circuit diagram is shown in figure 6-1.

One of each three-phase clock pulses toggles the reference J-K flip-flop and simultaneously triggers the one shot. With no $V_{control}$ signal the one shot delays its J-K flip-flop by 90 degrees. Its output is integrated and forms the triangular waveshape which after inversion is in phase with the reference phase.

Applying a control signal of positive or negative polarity shortens or lengthens the output pulse of the one-shot such that the following J-K delivers a square wave which can be shifted ± 80 degrees.

The advantage of this circuit is that it not only avoids the comparators Z9A and Z9B and also the ramp generator Z6A and Z6B but also eliminates the "jitter" caused by fast comparators.

The control signal to the "one-shot" is generated by the phase detection circuit.



Note: Select R1 and C1 of one shot for 50% duty cycle when $V_{control} = 0$

Figure 6-1. Three-Phase Front End

SECTION 7

RECOMMENDATIONS

The following recommendations are made:

1. Design, build and demonstrate phase synchronization between a digital input reference signal and the sinusoidal output voltage.

2. Design and build the power stage with capacitor C across output as shown in figure 4-1.

3. Optimize and stabilize the breadboard.

4. Convert the breadboard into a chassis with plug-in boards.

5. Equip the single phase inverter with short-circuit protection.

6. Design the single phase inverter to run without auxiliary voltage sources.

7. Build two more single phase inverters.

8. Develop a full three-phase system.

9. Test the three-phase system with any one of the three phases failing.

SECTION 8

PROBLEM AREAS

During the study several problem areas were encountered. Below these problem areas are discussed.

a. Sensitivity of comparators:

The breadboard uses comparators with high gain and a fast slewing rate. Due to these inherent characteristics these comparators have a tendency to pass through an area of undetermined output state and it shows up as a jittering of the output voltage between low and high whenever a DC level is compared with a relative slow ramp waveshape. This is the case in our application.

A detailed description of this phenomenon is presented in Texas Instruments' book, "Linear and Interface Circuits Application 1974," under the section, "Comparators," page 103 to 111.

A solution to this and the following problem was found in the use of a "correct phasing assurance circuit." This circuit is discussed in paragraph 5.7.

b. Phase Flipping Sensitivity of the J-K Flip-Flops:

The above tendency of the comparators to cause a "jitter" has a severe impact on the following J-K flip-flops and causes unpredictable triggering. As a result a phase-flipping of 180° occurs randomly.

The solution to this and the above problem was found in the use of the "correct phasing assurance circuit."

c. Failure and Non-Performance of the Motorola MC4044 Phase Detector:

The initial design of the phase detector circuit (see paragraph 5.6) used the Motorola Phase-Frequency detector MC4044 which in one dual-in-line package "contains two digital phase detectors, a charge pump and an amplifier. Phase detector 1 is intended for use in systems requiring zero frequency and phase difference at lock." A strictly functional truth table is not available as it does not show all possible modes of operation. The "truth table" is useful for DC testing only.

After a thorough discussion with a Motorola applications engineer, we were convinced we were using the best suitable component.

In-depth testing of the unit in our circuit however disclosed that Motorola was not aware of some shortcomings in their unit and that the unit could not operate in our intended application. This fact was eventually confirmed by two Phoenix based Motorola specialists for this device and their admittance of not being aware of this shortcoming made us lose considerable development time and cost.

Our own design was then incorporated and though it required more components it did work very satisfactorily (see paragraph 5.6)

d. Current Spikes During the Non-Conducting Time of the Main Switches:

The main switches in the Inverter Power stage are Solitron 96SV107. At the operating collector current values the saturated current gain is greater than 15 and the transistor has high speed switching characteristics. These characteristics in combination with the self-regenerative base drive make the off-transistor sensitive to stray signals. In our breadboard the off-transistor was momentarily

turned on whenever the on-transistor was turned off. The resulting collector current spikes during the off time of the main transistor was unacceptable because of additional stress levels and increased losses.

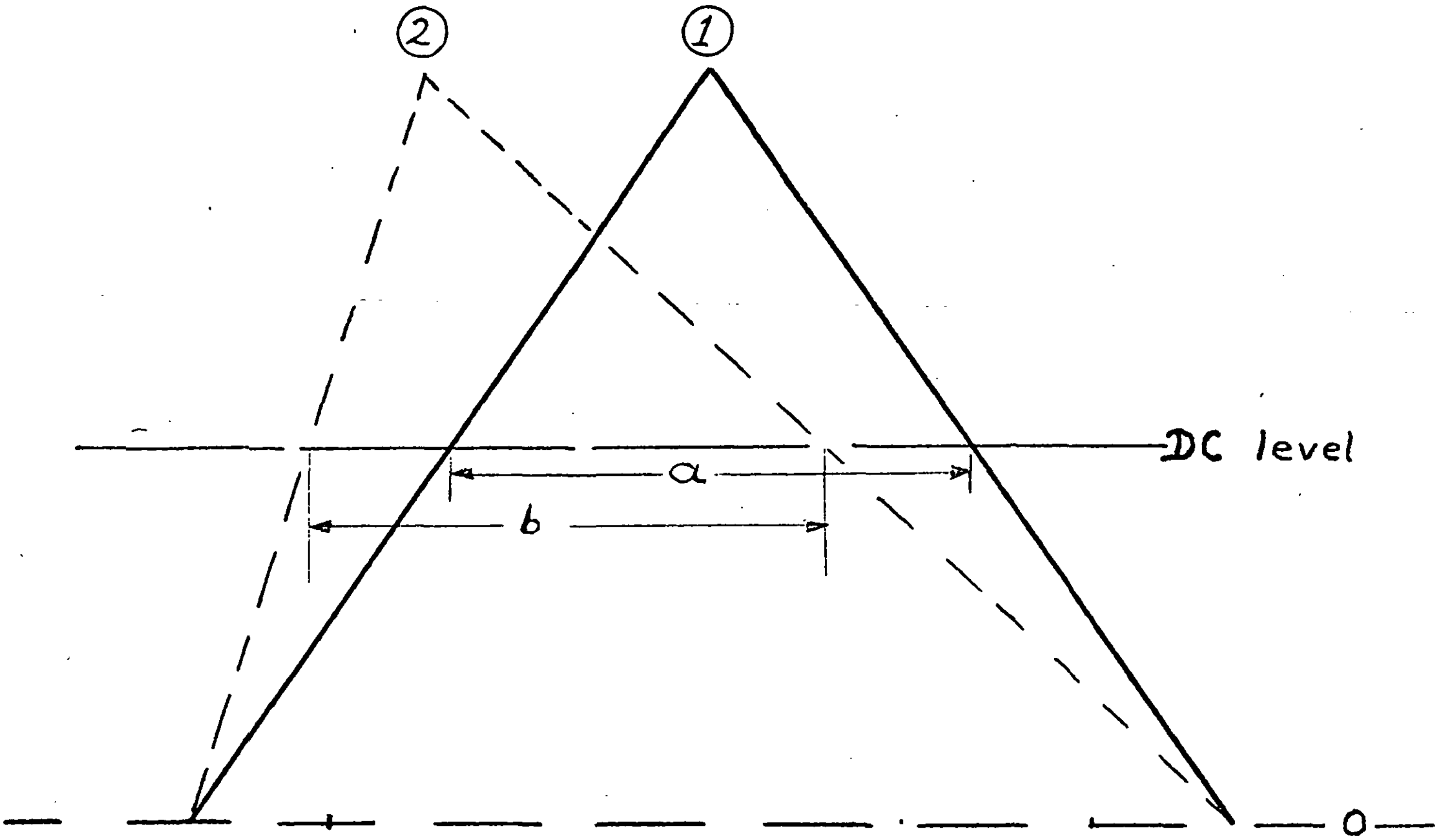
The problem was solved through the use of the "Active Off-Bias Circuit." (See paragraph 5.1)

e. Limitations of Another Phase Shift Approach Where the Apex of a Triangular Waveshape was Shifted Only:

With the advent of IC function generators it was attempted to use one of these devices to generate a triangular waveshape and at constant amplitude and frequency shift its apex through the application of a DC signal derived from the phase detector. Using a comparator and comparing a variable DC level with the triangular waveshape yields the desired pulsewidth modulation. As the attached figure 8-1 shows pulsewidth modulation ($a = b$) is independent from moving the apex from point 1 to point 2.

Figure 8-1 also illustrates that whereas the apex can be shifted $\pm 90^{\circ}$ any pulsewidth generated at a point lower than the apex can be shifted to a lesser degree. At a pulsewidth of 180° (DC level at 0) shifting of the apex no longer causes a shifting of the pulse location.

In the current-fed inverter pulse-shifting is required whenever a power factor is encountered. The question therefore arose: Does the narrowing of the pulsewidth as required by a power factor always keep the pulsewidth narrow enough so that enough room remains for pulse-shifting?



Pulse-width and phaseshift control through moving of apex of a triangular waveshape.

Figure 8-1.

A theoretical investigation revealed that this circuit would meet the requirements for a power factor of ± 0.7 as long as the turns ratio on the feed-choke $n_2 = n_1$ was equal to or greater than 5:1. This latter requirement however would force the inverter to always operate with narrow pulses, causing high switching currents, high RMS currents and low efficiency.

For these reasons this approach was therefore abandoned.

Successful operation was achieved with the circuit as described under paragraph 5-3.

All of the above problem areas were resolved during the breadboard study.

The following problems however remain unresolved due to limited time and funding and closing out of the program.

f. Stability Problems Under Certain Line, Load and/or Power Factor Conditions:

The incomplete test results indicated that the most severe stability problems occur under full load, capacitive power factors of 0.7 and high input voltage.

A full investigation into the stability problem is required.

g. Lack of Inductors:

The lack of suitable inductance values prevented measurements of fully rated inductive loading.

h. Low Output Voltage and Low Efficiency:

The magnetic components in the breadboard power stage use parts which out of necessity had to be available immediately and served well to prove the feasibility of this approach.

A redesign and optimization however is necessary to achieve the correct output voltage of 50V AC and improve the efficiency.

i. The Ability of the Single Phase Inverter to be Synchronized to an External Clock Signal was not Demonstrated:

This ability is one of the major requirements to assure not only single phase but also three phase operation, where any one phase may fail.

One solution to this problem is proposed in section 6-2.

SECTION 9

NEW TECHNOLOGY

1. Phase-lock technique for a current-fed inverter.

2. Phase detection and control circuit.

3. Correct phasing assurance circuit.

4. Three-phase adaptable front end.

5. Full wave perfect rectifier.

6. One hundred-eighty degrees clamp circuit.

7. Active off-bias circuit.

APPENDIX

1. THE CURRENT-FED INVERTER

2. DESIGN DATA FOR INDUCTOR-TRANSFORMER TI, FEED-CHOKE L AND CAPACITOR C

3. DERIVATION OF EQUATION FOR MINIMUM INDUCTANCE

4. WINDING INFORMATION FOR BREADBOARD INDUCTOR-TRANSFORMER TI AND FEED-CHOKE L

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THE CURRENT-FED INVERTER

A NEW APPROACH AND A COMPARISON WITH THE VOLTAGE FED INVERTER

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Static inverters are generally defined as devices that convert DC electrical power into AC electrical power and that contain no moving parts. Most of the circuits used today were developed about 30 years ago at which time low voltage inversion was impractical due to high forward drops in the available switches (Thyratrons, Electron Tubes, Mercury Rectifiers). With the advent of semiconductor switches, however, interest in inverters was drastically revived.

In most of today's inverter circuits an approach is used which I call the "Voltage-Fed Inverter." A power source is connected through a pair of switches into the ends of a centertapped transformer, as shown in Figure 1.

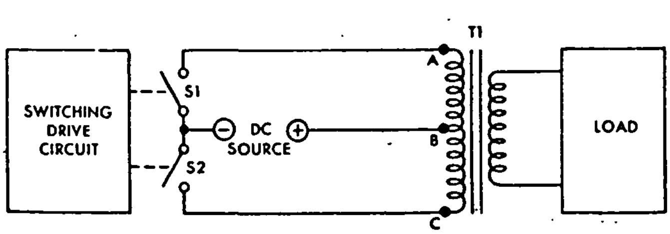


Figure 1. Basic Voltage-Fed Inverter Circuit.

We can now define the Voltage-Fed Inverter as follows:

"A Voltage-Fed Inverter is *any* inverter in which the design of the circuit connects the DC voltage through the switches, *directly* to the primary of the transformer."

This means, that when S1 is closed, the full DC source voltage (minus switch losses) will appear across the A-B primary of the transformer T1, and conversely when S2 is closed, the full source voltage will appear across the B-C primary. In this case, as in any other Voltage-Fed Inverter, the voltage impressed on the transformer during the time one switch connects the DC source to the transformer, is equal to the DC source voltage (switch losses neglected). This fits the definition for the Voltage-Fed Inverter: "The DC source *voltage* is impressed into the transformer."

The Effect of Power Factor

To simplify considerations let us consider the inverter as

shown in Figure 1. Switches S1 and S2 are opening and closing alternately and the resulting voltage waveform is a square-wave. Under a pure resistive load, voltage and current waveform are in phase (Figure 2). Under purely inductive load, however, the current waveshape becomes triangular and is shifted 90 degrees.

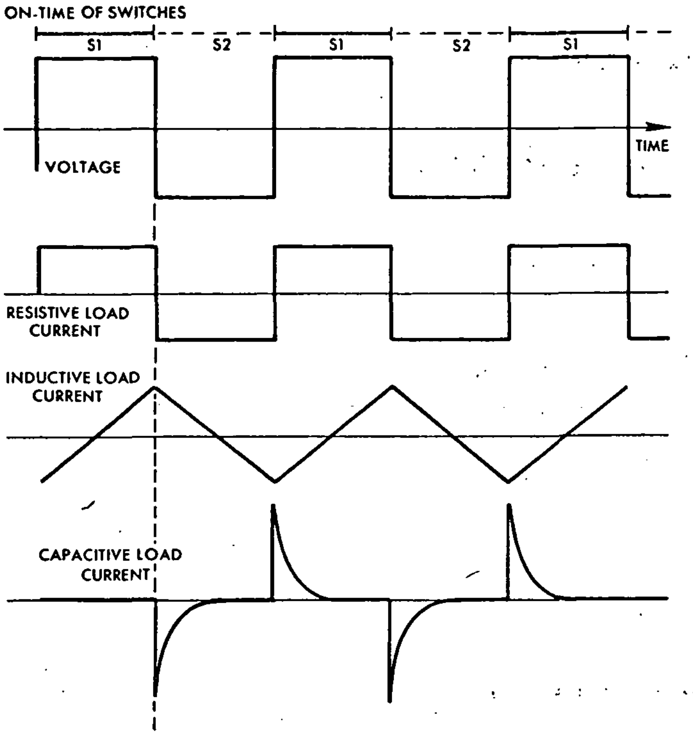


Figure 2. Voltage and Current Waveforms for Resistive, Inductive, and Capacitive Loads.

As the voltage waveshape is fixed with relation to the switching sequence, *the current-wave-shape must phase-shift* with respect to the switching sequence in order to accommodate power factor loads, thus establishing another characteristics common to all Voltage-Fed Inverters. Inspecting the inductive current waveshape Figure 2 also reveals, that during the time period that Switch S1 is closed, the inductive current flows both negative and positive. All of our semiconductor switches, however, are unidirectional in current flow and cannot handle negative currents as required by power factor loads. This causes the conducting time of the switches to be considerably shorter than the on-time. In order to deliver the same VA, peak values and RMS values of current must increase rapidly. Poor utilization of switches and necessary overdesign of transformer windings, therefore, are another characteristic of a Voltage-Fed Inverter.

Because the negative current required by inductive load, cannot be carried by semiconductor switches, it is necessary to establish another path. Two approaches are commonly used. The first one utilizes the more efficient approach of feeding the inductive energy through diodes back into the DC source, whereas the second approach, commonly used in low power applications, destroys the stored inductive energy in "De-Spiking Networks," RC combinations or plain dummy load resistors. It is interesting to note that the energy-feedback period is not regulated by any control loop.

Figure 2 also shows the current-waveshape under purely capacitive load conditions. The conduction time of the switches is now much shorter than the on-time. Very poor utilization of switches, increased RMS currents and necessary overdesign of transformer windings are the characteristics of a Voltage-Fed Inverter under capacitive loads.

Regulation and Filtering

The simple square-wave inverter used as illustrative example in Figure 1 is not always typical of the Voltage-Fed Inverters that are often seen in use. Some of the Voltage-Fed Inverters become more complex and utilize step-function three phase circuitry or other innovations that make them look different. It should be remembered that the definition of a Voltage-Fed Inverter is: "*Any* inverter in which the DC voltage source is connected through the switches directly to the primary of the transformer."

Because all basic characteristics explained for the sample square-wave inverter hold true for any Voltage-Fed Inverter, let us continue our consideration of the square-wave inverter, example in Figure 1.

One of the most effective methods of regulation is pulse-width-modulation. With increasing output voltage the on-time of the switches is reduced and the impressed voltage on the transformer becomes a semi-square wave. We are, therefore, looking at a *voltage* pulse-width-modulation (Figure 3).

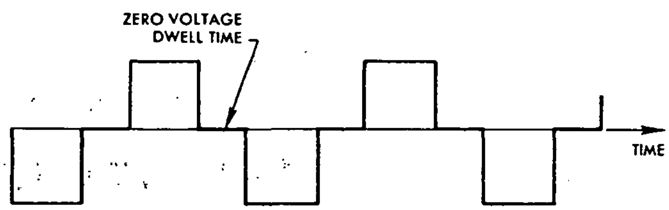


Figure 3. Pulse-Width Modulation in a Voltage Wave-Shape.

Regulation can be achieved by this means, however, there are some drawbacks. Any transformer operating from AC voltages with no zero-voltage dwell time changes its flux density level from a negative to a positive maximum and traverses the BH loop during the positive half-wave from point 1 through point 2 to point 3 and during the negative half-wave from point 3 through point 4 back to point 1.

Operating from a semi-square wave with its zero-voltage

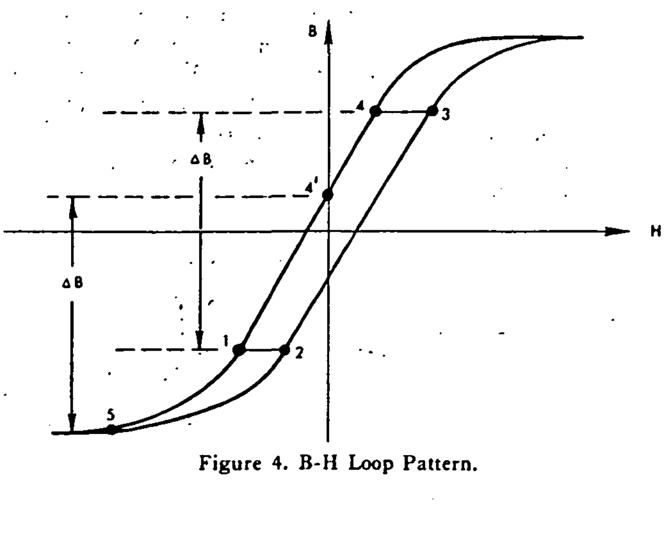


Figure 4. B-H Loop Pattern.

dwell time, and with the same average voltage, the BH loop pattern changes although the integral of the voltage K/EDT stays the same (therefore, ΔB remains the same). Let us assume that when we apply the positive half of the semi-square wave, the BH loop starts at point 1. At the end of the positive half-wave, the flux density is at point 3. During the zero-voltage dwell time, the core resets through 4 to 4'. The negative half-wave which follows requires the same ΔB. This forces the core into saturation at point 5. This is one of the reasons why voltage-pulse-width-modulation in the Voltage-Fed Inverter is seldom used. It forces the designer to a lower useful flux density, and increases weight.

Another problem is also created by the semi-square wave, generated by voltage pulse-width-modulation. It becomes apparent when we consider filtering the output of the transformer to generate a sine wave.

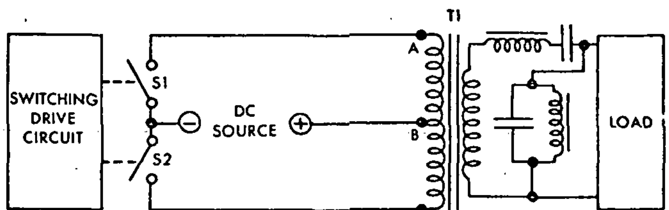


Figure 5. Basic Voltage-Fed Inverter with Filters.

During the dwell-time of the semi-square wave, only the magnetizing current of the transformer can flow. This interrupts proper filter operation. Larger filters are required to overcome this drawback. This is another reason for avoiding the use of voltage pulse-width-modulation in Voltage-Fed Inverters. A short summary lists the characteristics of typical Voltage-Fed Inverters:

1. Voltage held fixed (in phase) relative to the switch on-time.
2. Under power factor condition:
   current is shifting with respect to switch on-time;
   negative current cannot be carried by switches;
   conduction time shorter than on-time of switches;
   peak and RMS current increased, and poor utilization of switches and transformer.
3. Voltage pulse-width-modulation:
   lowers useful flux density of transformers, and decreases efficiency of filters.

The Current-Fed Inverter

A schematic presentation of the current-fed inverter is illustrated in Figure 6.

For purposes of our discussion, let us assume that Inductor L1, commonly called the feed-choke, is an inductance of sufficient value to maintain a constant current flow through

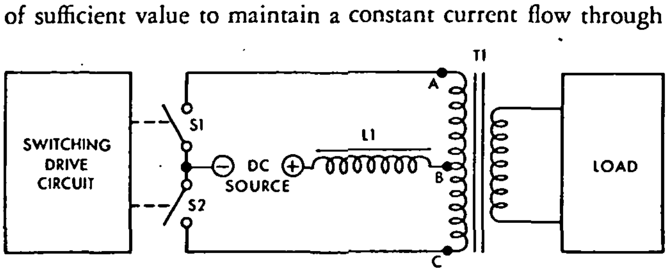


Figure 6. Basic Current-Fed Inverter Circuit.

the circuit under all conditions. The current flow, once established, tends to resist any change in current level and, therefore, *different* from the Voltage-Fed Inverter, the current through the switches and through the primary of the Transformer T1 is maintained as a square-wave of constant value no matter how the source voltage varies, no matter what the load and no matter what the power factor. Conduction time is always equal on-time of the switches.

If we feed a square-wave of current into a transformer with a resistive load on the secondary, we get a square-wave as output voltage. If the load, however, consists of capacitors only, the output voltage waveshape is triangular and shifted 90° with respect to the on-time of the switches and to square-wave of the current into the transformer. This illustrates one very important characteristic of the current-fed inverter: the *current-waveshape* from the source is always in phase with the on-time of the switches and the *voltage* of the transformer is phase-shifting with reference to the on-time of the switches, whenever a power factor is encountered.

It becomes obvious, that so far, the output *voltage* waveshape is influenced by the load and its power factor. (In the Voltage-Fed Inverter, the *current* waveshape from the DC source was influenced by the load and its power-factor) A simple addition to the circuit in Figure 6, however, changes this situation drastically. In Figure 7, a parallel resonant circuit, tuned to the natural frequency of the inverter, has been added across the secondary.

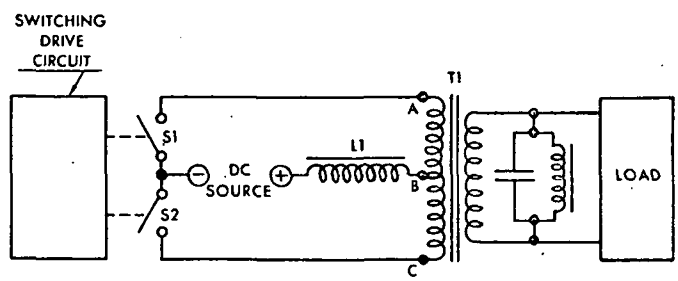


Figure 7. Current-Fed Inverter Circuit with Parallel Resonant Output Circuit.

With proper design the output voltage now is always a sine wave. This is accomplished by the parallel resonant circuit acting as a flywheel and waveshaping circuit, and by the feed-choke isolating the pulsing DC voltage from the sine wave across the primary of the transformer. Under no-load condition, only the losses need to be restored in the parallel resonant circuit. Any degree of sine wave purity can be achieved. It can also carry any power factor from zero leading to zero lagging without preloading.

Because the current waveshape is fixed, the voltage is phase-shifting and this causes the blocking voltage across the switches to become positive and negative. A silicon controlled rectifier can block these voltages, and a transistor switch can be aided by a series diode, in blocking the reverse voltages.

Regulation and Short-Circuit Protection

With the Feed-choke L1 connected as shown in Figure 6 and Figure 7, pulse-width-modulation of the current flow is impossible; the feed-choke would resist any interruption of current and destroy the switches. All that is needed to prevent the feed-choke from spiking is a method of maintaining

the proper current flow, or more precisely maintaining ampere-turns. This can readily be accomplished by adding a secondary winding to the feed-choke and connecting it, with proper polarity, through a diode to the DC source (Figure 8).

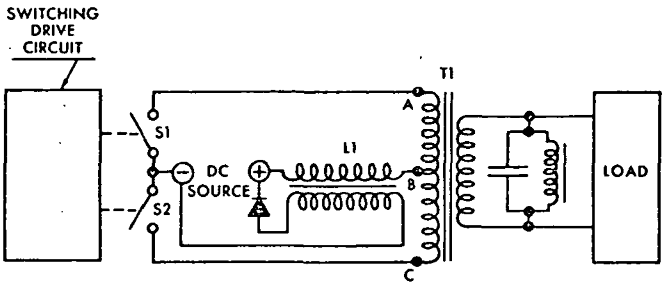


Figure 3. Current-Fed Inverter Circuit with Split Feed Choke.

Whenever both switches are open, the secondary of the feed-choke feeds stored energy back into the DC source, thus preventing any spiking.

Current pulse-width-modulation can now be used to control the output voltage of the inverter. The output voltage stays sinusoidal during the dwell time of the energizing current pulses. The parallel resonant circuit acts like a flywheel and maintains the sine wave of the output voltage. With current pulse-width-modulation, the output voltage can be regulated down to zero, at which point, the conduction time of the switches is not zero, but approximately 60° electrical. The firing angle at which the output voltage becomes zero, is controlled by the turns radio of the feed-choke. This characteristic of the current-fed inverter can be used in overload and short-circuit protection. It explains why the current-fed inverter is not shut-off, but is still operating when it encounters short-circuits.

Electro-Magnetic Interference and Audible Noise

Electro-magnetic interference is mostly generated by current spikes. Because the feed-choke does not generate spikes and the transformer with the parallel resonant circuit does not generate spikes, it is understandable that the current-fed inverter is not a generator of electro-magnetic interference.

The current-fed inverter circuit also becomes less of a problem from the viewpoint of audible noise. Most audible noise is created in the magnetics by magnetic flux forces, driven by the current waveshapes. The force waveshapes created in the magnetics of the Voltage-Fed Inverter contain a large percentage of higher harmonics, that results in a higher level of audible noise with a broad spectrum of frequencies.

The current-fed inverter, with its nearly sinusoidal waveshapes, therefore, creates less audible noise. We can now summarize the characteristics of the current-fed inverter:

1. The energizing current is held fixed (in phase) relative to the switch on-time.
2. Under power factor conditions:
   the transformer voltage is shifting with respect to the switch on-time;
   negative voltage can be blocked by the switches; conduction time is always the same as the switch on-time; and during the on-time, the current is constant through the switches, and is not affected by load.
3. Best possible utilization of switches and transformer winding.
4. Output voltage waveshape is sinusoidal.
5. Current pulse-width-modulation very efficient for regulation.
6. Inherent short-circuit protection.
7. Can handle any power factor without preloading.
8. Complexity of circuit less than in a Voltage-Fed Inverter. A typical three phase Voltage-Fed Inverter has 500 components whereas the three phase current-fed inverter of same capabilities has 140 components.

Conclusion

In the inverter discussion contained in this paper, I do not intend to imply in any manner, that the current-fed inverters are the "cure-all" for the problems that have plagued the development of the static inverter. The current-fed inverter has, however, overcome some of the major problems encountered in the voltage-fed inverters, such as power-factor handling, radiated and conducted EMI, audible noise, and complexity.

Acknowledgement is made to Mr. Robert Ferraez, Manager of Special Products, ITT Industrial Products Division, for his assistance in the preparation of this paper.

DESIGN DATA FOR INDUCTOR-TRANSFORMER, TI, FEEDCHOKE L AND CAPACITOR C

During the design-construction period it was of utmost importance to avoid delivery times and nonproductive high labor costs. After the initial design of the magnetic components and the capacitor value of the power stage as per schematic figure 4-1 it became immediately clear that the desired magnetic cores and the capacitor C had long delivery times. To avoid any delay it was therefore decided to use those magnetic cores which were available and were reasonably close to the desired values. For the capacitor C only 2μF values were available. To meet the required capacitive VAR rating the capacitors were therefore connected across a step-up winding as shown in figure 5-1. Furthermore the capacitors were split and connected across primary and secondary winding. This latter approach was taken to suppress any potential voltage spikes across the primary winding.

For reasons of expediency the actual power stage differs from the one shown in figure 4-1. It is however intended and recommended to use during the optimization of the design the circuit approach as shown in figure 4-1. For this design approach the following calculated values are presented.

For the design of the inductor-transformer TI and the feed-choke L with a turns ratio of $n_1:n_2 = 1:2$ the highest RMS values and the highest peak current values occur at a power factor of $\cos\varphi = 0.7$ and at the highest input voltage of E = 50V DC. The regulated AC voltage across one half of the primary of TI is assumed to be e_{12} = 25V AC.

Inspection of figure 4.3 yields a firing angle $\alpha = 47.1^\circ$ at a power factor of $\cos\varphi = 0.7$ and a ratio of $\frac{e_{12}}{E} = 0.5$. Equation -2 then yields the peak DC current

$$I = \frac{W}{2\,\hat{e}_{12}\,\cos\alpha\,\cos\varphi} = \frac{140.\,\pi}{2\sqrt{2}\;25 \times 0.68 \times 0.7}$$

$$I = 13.05 \text{ A}$$

$$\alpha = 47.1^{o} = 0.82 \text{ radians}$$

(-6) $$i_{RMS_{12}} = I\sqrt{\frac{\pi - 2\alpha}{2\pi}} = 6.38 \text{ Ampere}$$

The resonance capacitor C_{res} can be calculated per equation

(-9) $$C_{res} = \frac{2}{\omega\, R_{load_{min}}} \qquad \text{where } R_{load_{min}} = \frac{e^2_{out}}{P_{max}} = \frac{50^2}{200} = 12.5\Omega$$

$$C_{res} = 10.61\ \mu F$$

and

$$i_c = e_{out}\omega C = 50\cdot 2\cdot\pi\cdot 2400 \times 10.61 \times 10^{-6} = 8.00 \text{ Amp.}$$

$$i_{out} = \frac{P}{e} = \frac{200}{50} = 4.00 \text{ Amp.}$$

The RMS current on the secondary of TI is (worst case)

(-7) $$i_{RMS_{45}} = \sqrt{8^2 + 4^2 + 2\cdot 8\cdot 4\cdot 0.71} = 11.20 \text{ Amp}$$

The VA_{RMS} rating of inductor-transformer TI is then

-8

$$VA_{RMS_{TI}} = 2 \times 25 \times 6.38 + 50 \times 11.2$$

$$VA_{RMS_{TI}} = 879\ VA_{RMS}$$

The inductance of the secondary winding is

-10

$$L_{45} = \frac{1}{\omega^2 C_{res}} = \frac{1}{(2\pi\ 2400)^2 \times 10.61 \times 10^{-6}}$$

$$L_{45} = 414.5\ \mu H$$

The actual inductance of the output winding n_{56} is $52^2 \times 146 \times 10^{-9}$ = 395 μH and slightly less than the calculated value of 414.5 μH.

The inductor transformer TI has a step-up winding for the secondary capacitor and half of the resonance capacitance connected across the primary in order to achieve the required VAs of the capacitor. This however does not effect the required inductance of the output winding as long as the total reflected capacitance amounts to the calculated value of C_{res} = 10.61 μF. In the case of the breadboard capacitance the reflected value is:

$$C_{ref_1} = C_{prim} \frac{n_{13}}{n_{56}} + C_{sec} \frac{n_{47}}{n_{56}}$$

$$= 2 \times 10^{-6} \left(\frac{52}{52}\right)^2 + 2 \times 10^{-6} \left(\frac{110}{52}\right)^2 = 10.95\ \mu F$$

This value is also very close to the original calculated value of C_{res} = 10.61 μF.

NOTE:

As the present breadboard model was not built in accordance with figure 4-1 it is not an optimized design and the output ripple voltage is considerably higher than it would be if the output capacitor was connected directly across the output terminal. At the time of the design only two capacitors of 2 μF each were available without delay. To achieve twice the VAR rating (400 VAR) as the maximum power rating of 200W one capacitor was connected across the full primary winding and 50 VAC and the second capacitor was connected across a stepped-up voltage of 106 volts on the secondary winding of TI. Thus the total VAR of the capacitor was:

$$VAR_{total} = 50^2 \times 2 \times \pi \times 2400 \times 2 \times 10^{-6} + 106^2 \times 2 \times \pi \times 2400 \times 2 \times 10^{-6}$$

$$= 414$$

The actual total VA_{RMS} rating of the breadboard inductor-transformer TI is then:

$$\text{Secondary:}\quad 56^2 \times 2 \times \pi \times 2400 \times 2 \times 10^{-6} = 94.6$$

$$+\ 50 \times \sqrt{8^2 + 1.51^2 + 8 \times 1.51 \times 0.71} = \underline{432}$$

$$\text{Subtotal}\quad 526.6$$

$$\text{Primary:}\quad e_{13} \times \sqrt{i^2_{RMS_{12}} + i_c^2}$$

$$= 50 \times \sqrt{6.38^2 + 1.51^2} = \underline{327.8}$$

$$\text{Total } VA_{RMS} \text{ of TI} = 854$$

As this figure indicates there is only a small difference in the VA_{RMS} rating of TI if one compares the required VA_{RMS} of the intended design (879 VA_{RMS}) with the breadboard rating of TI (854 VA_{RMS}).

The feed-choke L was selected to have a turn ratio of $n_1:n_2 = 1:2$.

The inductance of the primary winding is designed so that it can maintain an uninterrupted current flow at 15 percent of the maximum load. At an AC voltage of $e_{AC} = 25$ volts across one half of the primary winding of inductor-transformer TI the minimum required primary inductance of L at a maximum load resistor of

$$R_{12_{max}} = \frac{e_{AC}^2}{0.15\ P_{max}} = \frac{25^2}{0.15 \times 200} = 20.8\Omega$$ is according to equation

-13 $$L_{min} = \frac{0.06R_{12_{max}}}{f} = \frac{0.06 \times 20.8}{2400} \quad [H]$$

$$L_{min} = 520\ \mu H$$

The actual value of the breadboard inductance is 536 μH.

At a peak current of $I = 13.05$ Amp and $\alpha = 47.1^\circ \hat{=} 0.822$ radians the worst case RMS current values are:

Primary Current:

-14 $$i_{RMS_{n_{12}}} = I \sqrt{\frac{\pi - 2\alpha}{\pi}} = 13.05 \sqrt{\frac{\pi - 2 \times 0.822}{\pi}} = 9.01 \text{ Amperes}$$

Secondary Current:

-15 $$i_{RMS_{n_{34}}} = I \frac{n_1}{n_2} \sqrt{\frac{2\alpha}{\pi}} = 13.05\ \frac{1}{2} \sqrt{\frac{2 \times 0.822}{\pi}} = 4.72 \text{ Ampere}$$

In conversion circuits which utilize an inductor as either a filter element or as an energy storage component it is generally desired to maintain an uninterrupted DC current at some specified minimum DC current I_{min} or at a maximum specified load resistor R_{max}. This condition is met if the minimum inductance L_{min} allows one half of the peak to peak value ΔI of the ripple current to become equal to the minimum DC current I_{min}

-1A

$$I_{min} = \frac{1}{2} \Delta I$$

The minimum DC current I_{min} is a function of the rectified AC voltage E_{av} and the maximum load resistor R_{max}

-2A

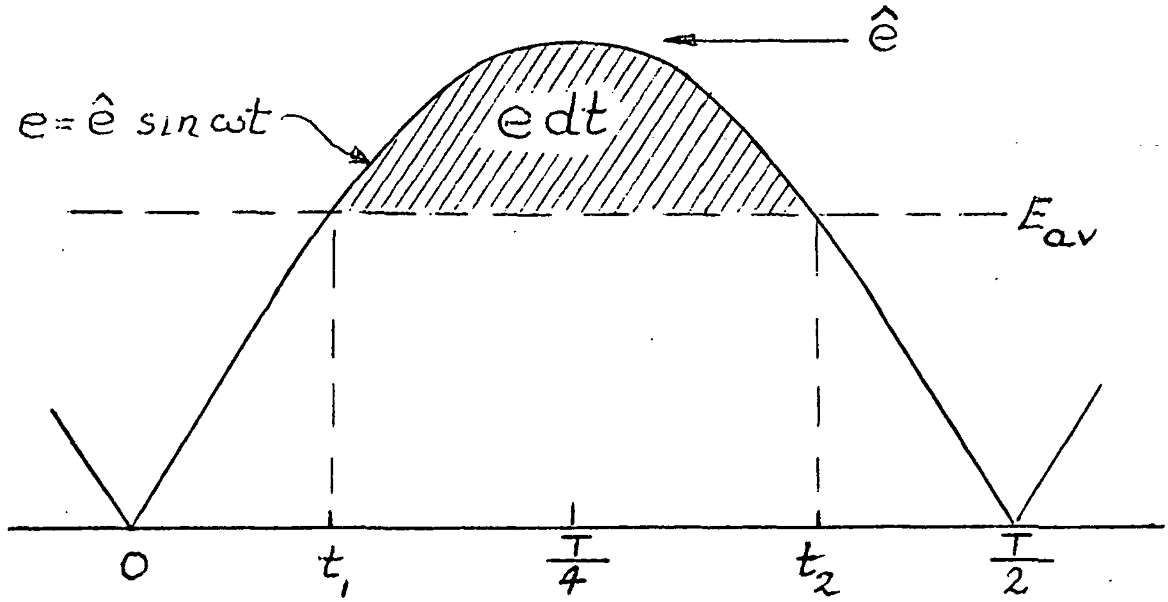
$$I_{min} = \frac{E_{av}}{R_{max}}$$

Figure A. shows a half cycle of a rectified AC voltage waveshape, where the average DC voltage E_{av} and the positive volt-seconds edt of the ripple voltage is shown as shaded area. It is this edt which causes the peak to peak ripple current ΔI in accordance with the following equation

-3A

$$\Delta I = \frac{edt}{L_{min}}$$

Combining equations -1A, -2A and -3A yields the equation which allows us to calculate the minimum inductance L_1 as a function of maximum load resistance R_{max} and carrier frequency f in Hertz [Hz]



One half cycle of a rectified AC voltage

Figure A.

$$\frac{E_{av}}{R_{max}} = \frac{1}{2} \frac{edt}{L_{min}}$$

-4A

$$L_{min} = \frac{1}{2} \frac{edt}{E_{av}} R_{max}$$

Inspection of figure 4-4 reveals that the expression $\frac{edt}{E_{av}}$ can be expressed as

$$\frac{edt}{E_{av}} = \frac{\hat{e}\int_{t_1}^{t_2} \sin \omega t \, dt - E_{av}\left(t_2 - t_1\right)}{E_{av}}$$

$$= \frac{\hat{e}\int_{t_1}^{t_2} \sin \omega t \, dt}{E_{av}} - \left(t_2 - t_1\right)$$

$$= \frac{\hat{e}\int_{t_1}^{t_2} \sin \omega t \, dt}{\frac{\hat{e}}{\frac{T}{2}}\int_{0}^{\frac{T}{2}} \sin \omega t \, dt} - \left(t_2 - t_1\right)$$

$$= \frac{\frac{\hat{e}}{\omega}\left(\cos \omega t_1 - \cos \omega t_2\right)}{\frac{\hat{e}\,2}{\pi}} - \left(t_2 - t_1\right)$$

-5A

$$\frac{edt}{E_{av}} = \frac{\frac{\hat{e}\,T}{2\pi}\left(\cos \omega t_1 - \cos \omega t_2\right)}{\frac{\hat{e}\,2}{\pi}} - \left(t_2 - t_1\right)$$

A comparison with the second equation in this derivation yields

-6A $$E_{av} = \frac{\hat{e}\,2}{\pi}$$

Further inspection of figure 4-4 reveals that due to symmetry

$$\frac{T}{4} - t_1 = t_2 - \frac{T}{4}$$

and hence

-7A $$t_2 - t_1 = \frac{T}{2} - 2\,t_1$$

Furthermore at the time t_1 the value of the sine wave $e = \hat{e} \sin \omega t$ is equal to E_{av}

$$\hat{e} \sin \omega t_1 = E_{av} = \frac{\hat{e}\,2}{\pi}$$

-8A $$\sin \omega t_1 = \frac{2}{\pi} \;;$$ -9A $$\omega t_1 = \sin^{-1}\left(\frac{2}{\pi}\right)$$

-10A $$\cos \omega t_1 = \sqrt{1 - \frac{4}{\pi^2}}$$

In combination with equation -7A

$$\cos \omega t_2 = \cos \left[\omega\left(\frac{T}{2} - t_1\right)\right]$$

$$= \cos \omega \frac{T}{2} \cos \omega t_1 + \sin \omega \frac{T}{2} \sin \omega t_1$$

-11A

$$\cos \omega t_2 = - \cos \omega t_1$$

Therefore

$$\cos \omega t_1 - \cos \omega t_2 = 2 \cos \omega t_1$$

-12A

$$\cos \omega t_1 - \cos \omega t_2 = 2 \sqrt{1 - \frac{4}{\pi^2}}$$

According to equation -7A

$$t_2 - t_1 = \frac{T}{2} - 2 t_1 \qquad \text{where } \omega \frac{T}{2} = \pi$$

-13A

$$t_2 - t_1 = \frac{\pi - 2 \sin^{-1}\left(\frac{2}{\pi}\right)}{\omega}$$

Inserting equations -12A and -13A into equation -5A yields:

$$\frac{edt}{E_{av}} = \frac{\frac{\hat{e}\, T}{2\pi} \times 2 \sqrt{1 - \frac{4}{\pi^2}}}{\frac{e\, 2}{\pi}} - \frac{\pi - 2 \sin^{-1} \frac{2}{\pi}}{\omega}$$

where $T = \frac{1}{f}$ and $\omega = 2\pi f$

$$= \frac{1}{f}\left(\frac{\sqrt{1 - \frac{4}{\pi^2}}}{2} - \frac{\pi - 2 \sin^{-1}\left(\frac{2}{\pi}\right)}{2\pi}\right)$$

-14A

$$\frac{edt}{E_{av}} = \frac{1}{f}\ 0.105256831$$

Inserting -14A into equation -4A yields the desired information for the design information for the minimum inductance

-15A

$$L_{min} = \frac{0.0526\ R_{max}}{f}$$

Adding a 15 percent safety margin yields the commonly used equation

-16A

$$L_{min} = \frac{0.06\ R_{max}}{f}\ ; \quad \text{see } \text{-13} \text{ on page 4-13.}$$

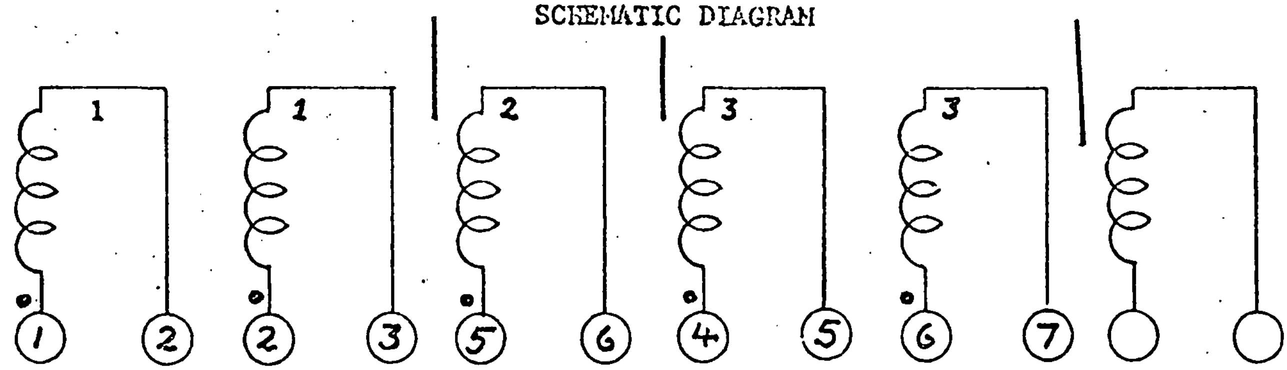
TOROID WINDING SPECIFICATION

PART NO.	
CHANGED FROM	
PAGE OF PAGES	
DATE	29 May 75
COMPILED BY	
ENGR	[signature]
REVISION	DATE

PART NO. Current-fed inverter, Inductor-transformer 200 VA output at 1∠0.5 PF and 56 VAC 2400 Hz. E_{in} = 25 to 50 VDC

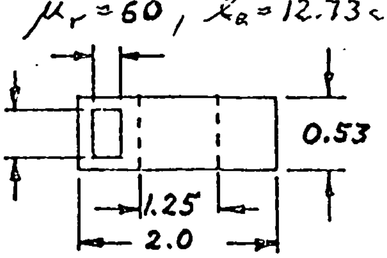
CORE 55716-A2	NO. REQUIRED 2	MATCHED TO				
MACHINE						
SHUTTLE NO.						
WINDING NO.	1	2	3	4	5	6
SINGLE(S) PAIR(P) TRIPLE(T)	P	P	P			
WIRE SIZE	15	16	18			
TURNS	–	52	–			
BIFILAR	26	–	29			
TAPS	–	–	–			
AVERAGE TURNS/LAYER	Wind evenly around core					
NO. OF LAYERS						
LAYER INSULATION						
WRAPPER WIDTH	1/2	1/2	1/2	50% overlapp on inside		
WRAPPER THICKNESS	EE 6379, 3 mil Permacel tape, Kapton-H					
LEADS (Self or Other)	Self		Self			
LENGTH (Out of Coil)	8"		8"			
LEAD WIRE SIZE	–		–			
LEAD INSULATION	–		–			
HIGH POT (Ref)						
COIL RESISTANCE						

SCHEMATIC DIAGRAM



NOTE: WIND ALL COILS IN SAME DIRECTION STACKED SAME

CORE DATA each
$\mu_r = 60$, $\ell_e = 12.73$ cm



P = 2×.226 (in^4)

Q$_{off.}$ 2×1.251 (cm^2)

Iron Wt 2×133 (grams)

LEAD NUMBER	1	2	3	4	5	6	7	8
PREFERRED	BRN	RED	OR	YEL	GRN	BLUE	PURP	GREY
ALTERNATE								
LEAD NUMBER	9	10	11	12	13	14	15	16
PREFERRED	WHT	BLK	BRN WHT	RED WHT	OR WHT	YEL WHT	GRN WHT	BLUE WHT
ALTERNATE								

PRODUCTION NOTES: Stack cores on top of each other. Then wind.
2μF across 1-3 and 2μF across 4-7 251

PART NO.	
CHANGED FROM	
PAGE OF PAGES	
DATE	3 June 75
COMPILED BY	
ENGR	
REVISION	DATE

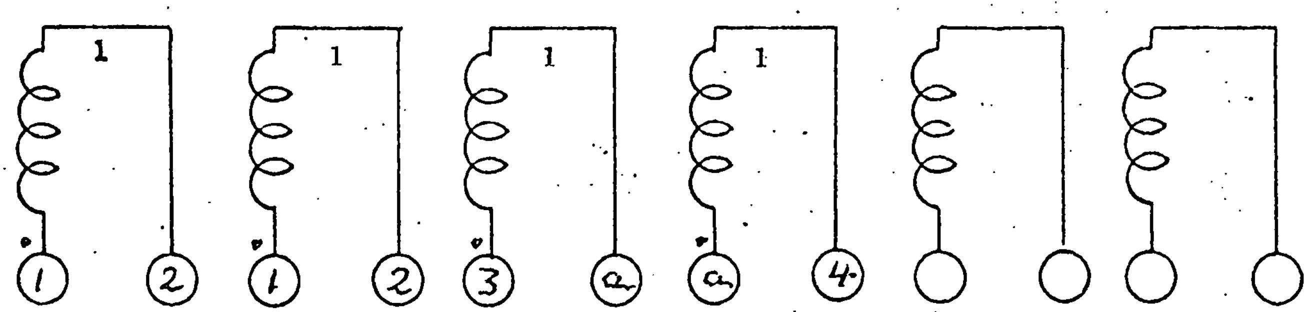
TOROID WINDING SPECIFICATION

PART NO. Feed-choke, Current-fed Inverter
200 VA output @ 1 ... 0.5 P.F and 56 VAC.
2400 Hz . E_{in} = 25 to 50 VDC

CORE 55715-A2	NO. REQUIRED 2	MATCHED TO				
MACHINE						
SHUTTLE NO.						
WINDING NO.	1	2	3	4	5	6
SINGLE(S) PAIR(P) TRIPLE(T)	P					
WIRE SIZE	16					
TURNS						
4-FILAR	42					
TAPS	—					
AVERAGE TURNS/LAYER	Wind evenly around cores					
NO. OF LAYERS	—					
LAYER INSULATION	—					
WRAPPER WIDTH	1/2"	50% overlapp on inside of toroid.				
WRAPPER THICKNESS	3 mil, Kapton H, Permacell EE 6379					
LEADS (Self or Other)	Self					
LENGTH (Out of Coil)	8"					
LEAD WIRE SIZE						
LEAD INSULATION						
HIGH POT (Ref)						
COIL RESISTANCE						

L_{1-2} = 536 μH

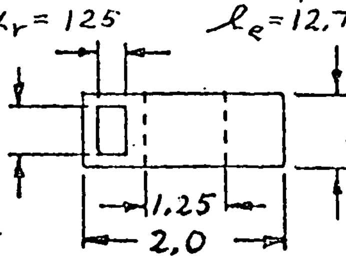
SCHEMATIC DIAGRAM



NOTE: WIND ALL COILS IN SAME DIRECTION STACKED SAME

CORE DATA, each

μ_r = 125 ℓ_e = 12.73 cm



P = 2 x 0.226 (in^4)

Q off. 2 x 1.251 (cm^2)

Iron Wt 2 x 133 (grams)

LEAD NUMBER	1	2	3	4	5	6	7	8
PREFERRED	BRN	RED	OR	YEL	GRN	BLUE	PURP	GREY
ALTERNATE								
LEAD NUMBER	9	10	11	12	13	14	15	16
PREFERRED	WHT	BLK	BRN WHT	RED WHT	OR WHT	YEL WHT	GRN WHT	BLUE WHT
ALTERNATE								

PRODUCTION NOTES: Stack cores on top of each other. Then begin winding.

252